Modularized, Reconfigurable and Bidirectional Charging Infrastructure for Electric Vehicles with Silicon Carbide Power Electronics (MoReSiC)

Deliverable D2.2 (Month 15)

Title: "Laboratory prototype of the SiC-based power electronics submodule"

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Executive summary

This deliverable is focused on the laboratory prototype of the Power Electronics Submodule (PES) designed earlier in the work package. The document showcases the constructed universal circuit to be used as a basis for all the converters in the MoReSiC system. Furthermore, the single-phase test setup used for the prototype verification is shown, and a thorough experimental study investigating the operation of the PES: the module's switching performance, efficiency, and thermal aspects have been considered. Ultimately, the prototype is successfully validated, as PES reaches all aims.

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1. Power Electronics Submodule (PES) prototype

The laboratory prototype of the SiC-based Power Electronics Submodule (PES) is the core part of the fast-charging system, being the base for all the converters. To briefly recap the layout of the PES from the previous task, the submodule is based on the ANPC structure, built exclusively from 6 SiC power MOSFETs. In order to reach the required 1500 V DC blocking voltage in a three-level structure, state-of-the-art NTH4L040N120SC1 with 1200 V/40 mΩ SiC power transistors are used. The power circuit was designed with the minimization of the conduction loops in mind to reduce the power losses, and improve the switching performance, e.g., through the minimization of the voltage ringing and overshoots harmful to the system. This was achieved through a 4-layer power board structure and a highly compacted power device layout. Furthermore, the heatsink Fischer LAM 6 with forced-air cooling is used to provide satisfactory junction temperatures of the devices and manageable heatsink temperatures. Moreover, the bipolar DC-link is supported by two main DC capacitors rated at 800 V and 60 µF. Finally, the submodule also consists of self-made gate drivers based on Texas Instruments UCC21750 integrated circuit, providing satisfactory switching capabilities, along with protection measures in case of a fault or a malfunction within a compact footprint, so that safety is assured, both for the submodule itself, and the full converters.

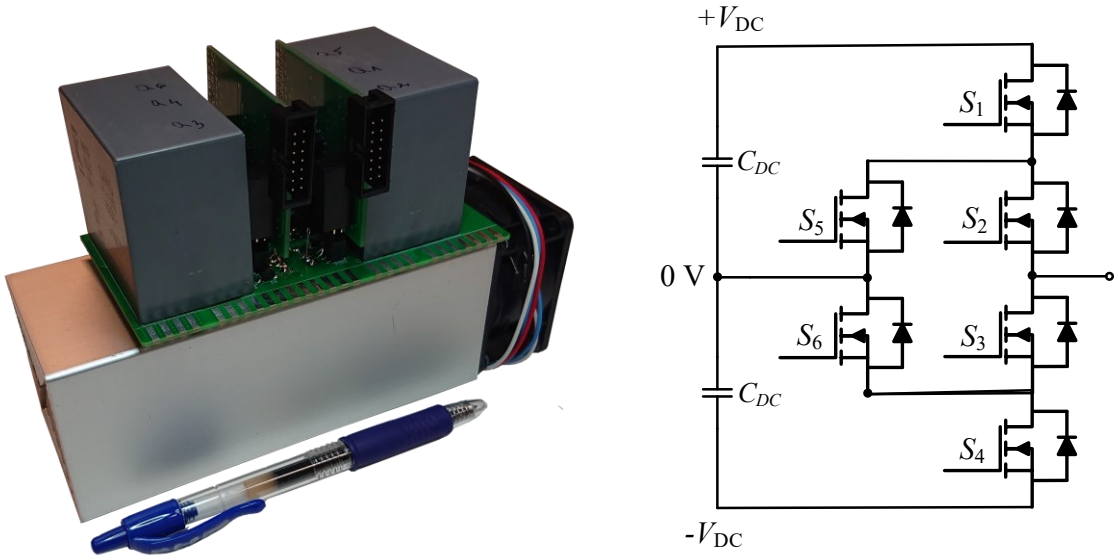


Figure 1 – The laboratory prototype of the SiC-based power electronics submodule: a) photo, b) scheme.

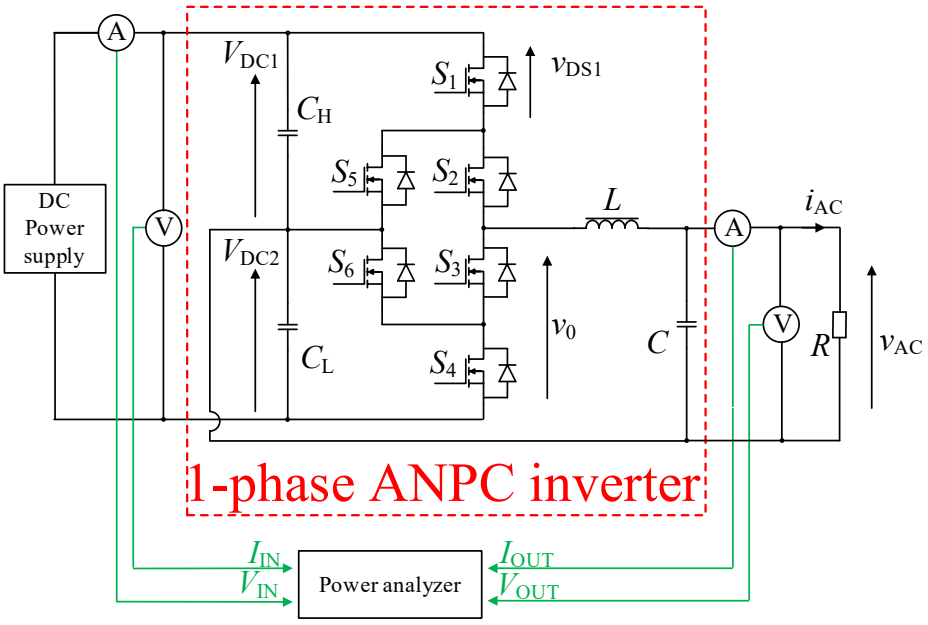
2. Single-phase test setup

In order to test the performance of the power submodule and simply validate the design, a single-phase inverter configuration was employed. Furthermore, such topology is favorable, as the conditions for the power submodules are similar to those expected in the three-phase inverter system. Here, in addition to the power submodule block, the DC-link was supported with 2 x 550 µF capacitors, leading to a total capacitance of 2 x 610 µF, as in the single-phase setup, in opposition to a three-phase system considered further in the project, excessive voltage fluctuation at the DC-link are expected. Furthermore, an LC filter with 220 µH and 4.7 µF was used to ensure sinusoidal currents. The switching frequency was set to 64 kHz, and a resistive load was used. The summarized parameters are presented in Table 1.

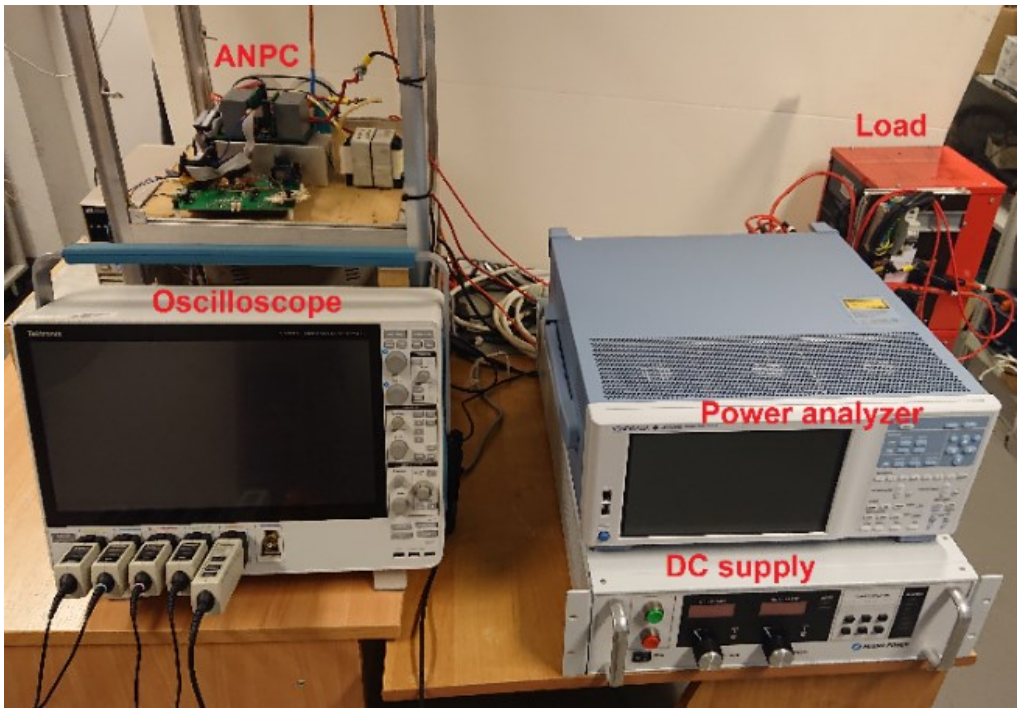
Table 1 – Parameters of the single-phase test system

Parameter	Description
DC voltage	1500 V
AC voltage	230 V RMS/50 Hz
Rated power	6.67 kVA (1/3 of 20 kVA)
Operating frequency	64 kHz
SiC MOSFETs	NTH4L040N120SC1
Filter inductor	220 µH
Filter capacitor	4.7 µF
DC capacitors	2 x 610 µF

Moreover, the system was controlled in an open-loop configuration for the sake of simplicity, and several modulation techniques known from the literature were tested (here, named PWM1 – 4). Finally, the test setup also contained the DC supply from Magna Power (2 kV/10 kW), oscilloscope Tektronix MSO6, and Yokogawa WT5000 power analyzer. The scheme and the photo of the experimental setup are shown in Fig. 2.



a)



(b)

Figure 2 - Experimental setup for the validation of the PES through an ANPC single-phase inverter system with a resistive load – (a) scheme, (b) photo.

3. Experimental results

Exemplary experimental waveforms obtained at 1500 V DC and 6.5 kW power (m = 0.45, v_{AC} = 230 V) are depicted in Fig. 3. As can be seen, the performance at the nominal inverter operating point was satisfactory. A specific imbalance in the DC-link voltages affecting the results can be noted, a usual trait for single-phase inverter systems. However, it was not crucial for the validation of the power submodule and thus was left out. Furthermore, the transistor switching waveforms, both for turn-on (a) and turn-off (b), are depicted in Fig. 4 for the positive load current and Fig. 5 for the negative load current. Unfortunately, due to the highly compacted design of the submodule, aiming at the minimization of stray inductances and improving the switching process of the switches, measuring the transistor currents was impossible. Nevertheless, based on the drain-source voltage waveforms, the switching performance is good, with relatively low voltage oscillations and overshoots. Furthermore, it should be noted that the depicted switching transitions were observed for the modulation with the highest ringing, while other modulation types exhibit lower ringing - for more specific voltage overshoot values for different modulation techniques, please refer to Table 2.

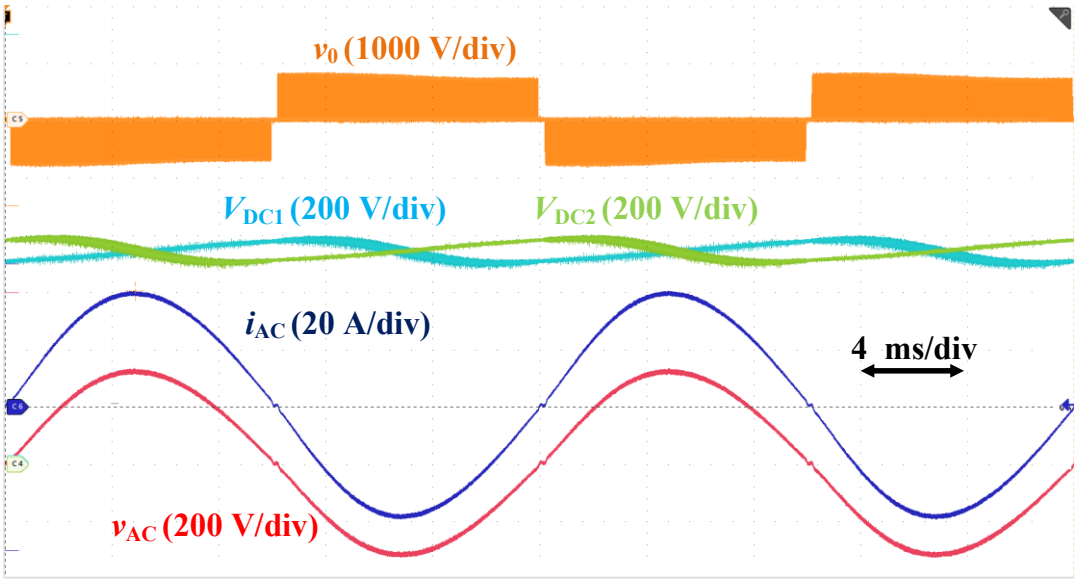


Figure 3 - Experimental results from a test at 1500 V DC and 6.5 kW power (m=0.45, v_{AC}=230 V) – line frequency-focused view. From the top: ANPC leg output voltage v_0, DC-link voltages V_{DC1} and V_{DC2}, load AC voltage v_{AC} and current i_{AC}.

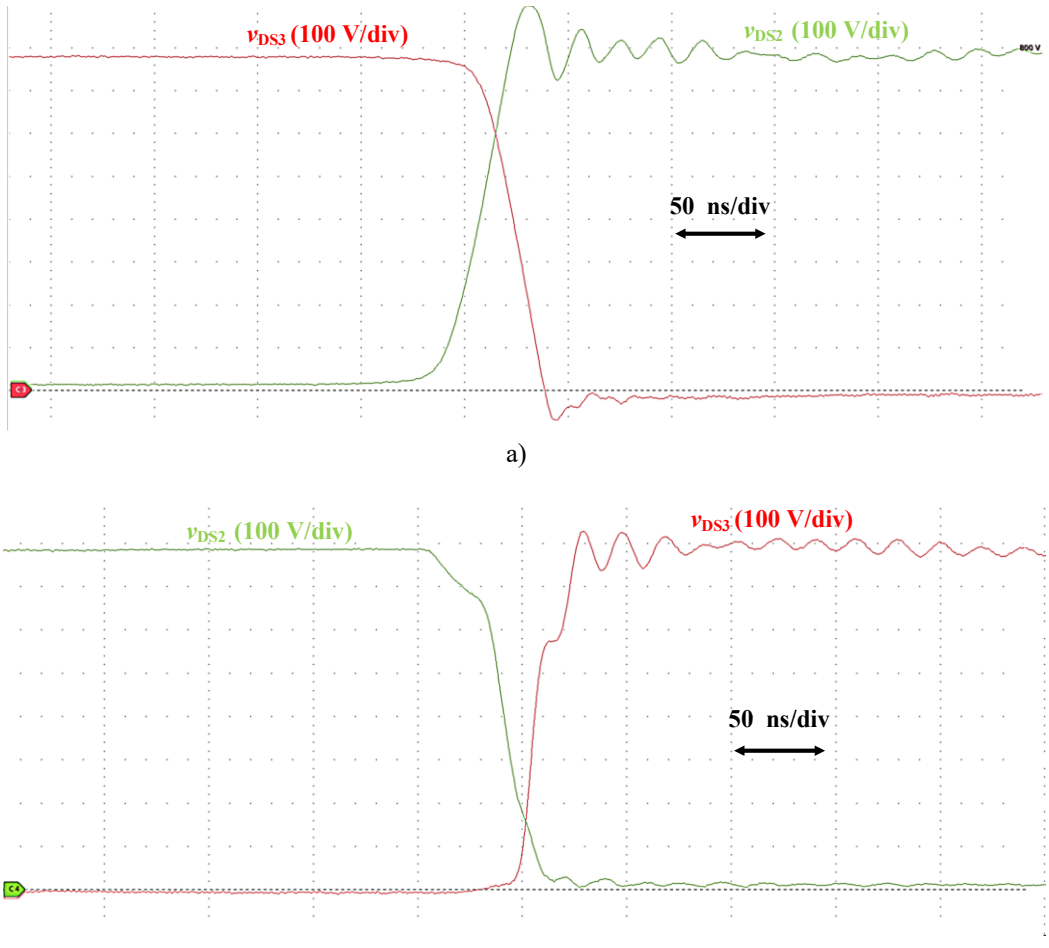


Figure 4. Exemplary experimental waveforms showcasing drain-source transistors for positive load current (i_{AC} > 0) for the modulation technique with highest overvoltages (PWM2) – (a) turn-on, (b) turn-off.

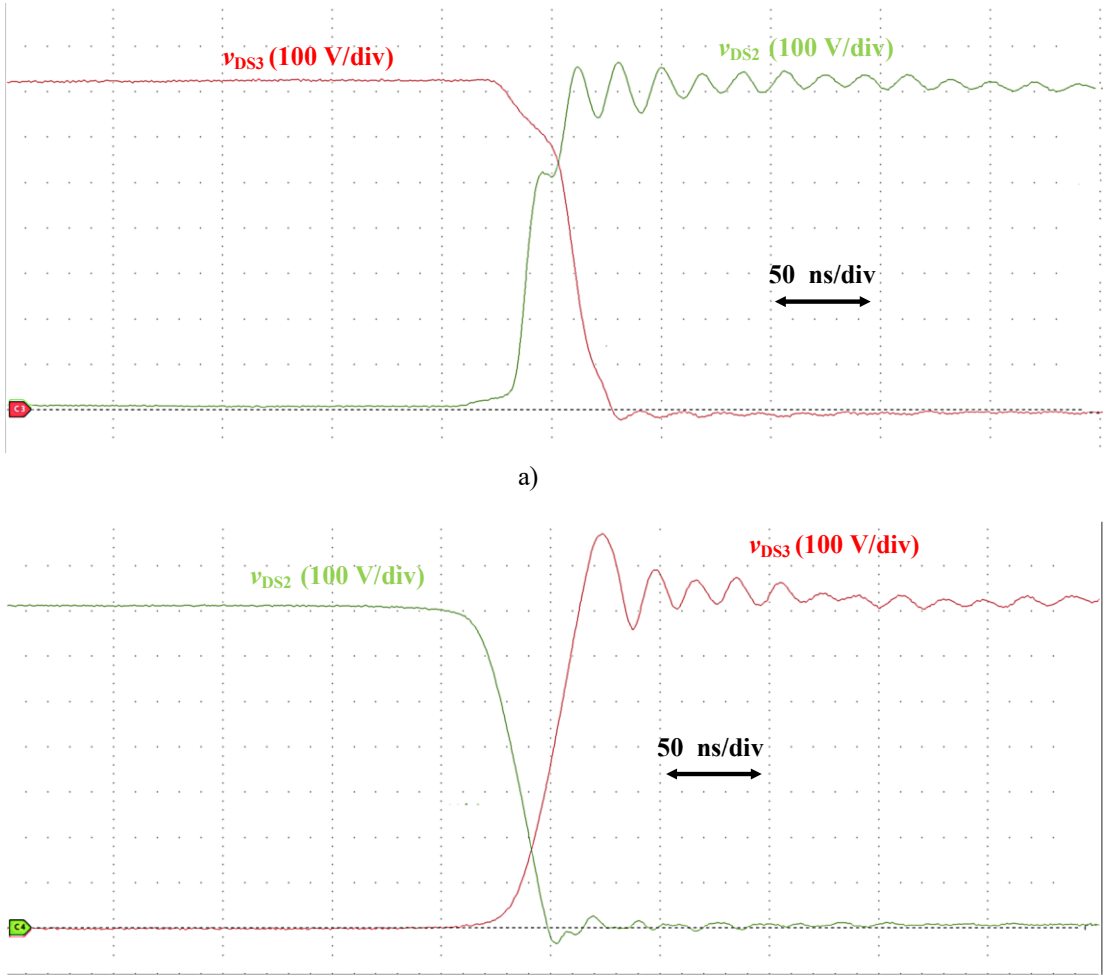
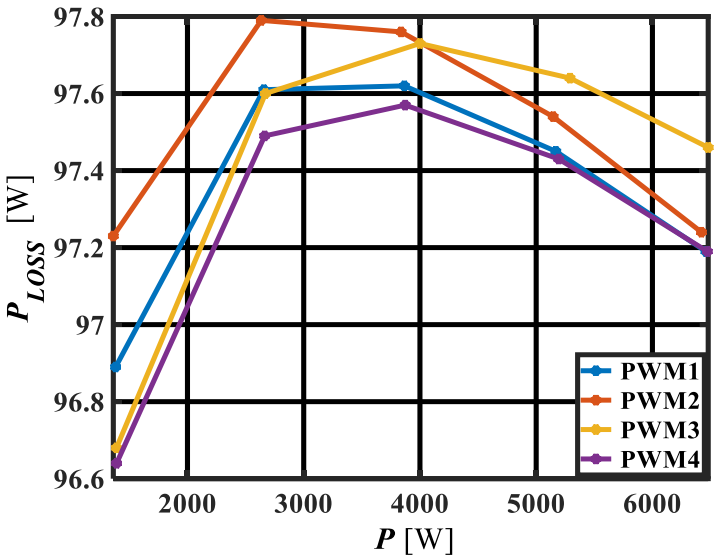


Figure 5. Exemplary experimental waveforms showcasing drain-source transistors for negative load current ($i_{AC} < 0$) for the modulation technique with highest overvoltages (PWM2) – (a) turn-on, (b) turn-off.

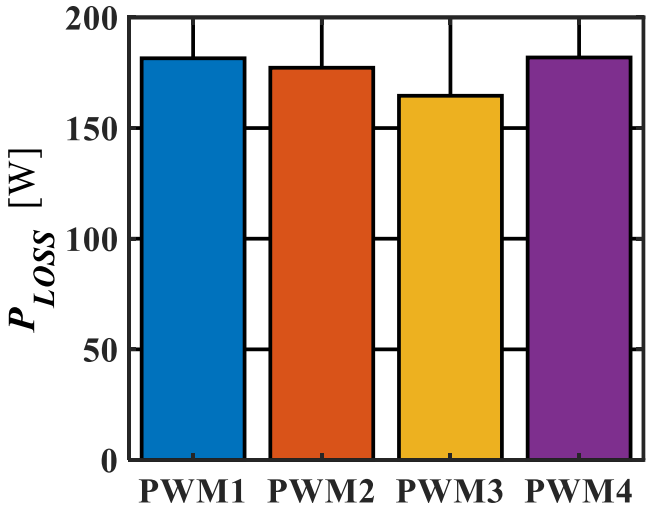
Table 2. Transistor voltage overshoots for the different modulation patterns at nominal ratings of the ANPC leg.

V_{DC} = 1500 V; P = 6.5 kW; v_{AC} = 230 V rms				
Parameter	PWM1	PWM2	PWM3	PWM4
$v_{DS\_max(S3)}$ [V]	832	957	846	827
$v_{DS\_max(S4)}$ [V]	889	802	868	873
$v_{DS\_max(S6)}$ [V]	857	848	842	843
$P_{LOSS(exp.)}$ [W]	182	177	165	182

Moreover, to establish the efficiency and further validate the power submodule design, the power losses were also measured using the power analyzer. The power loss values measured for the nominal point of 6.5 kW and 1.5 kV for the different modulation techniques are also exhibited in Table 2 and Fig. 6b, while the efficiency characteristics obtained for a wide load range are depicted in Fig. 6a. As can be seen, the obtained values are notable for such a low modulation index (m = 0.45).



(a)

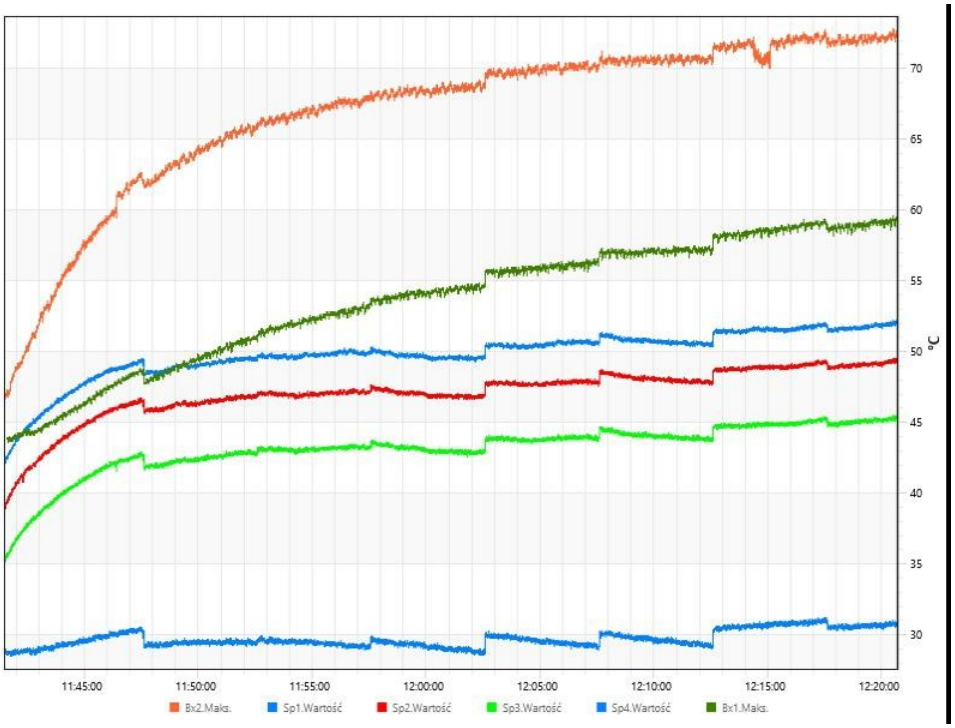


(b)

Figure 6. Experimental characteristics showcasing the performance of the ANPC leg in the function of converter power P – (a) efficiency, (b) power loss at the nominal operating point (1500 V DC, 6.5 kW).

Furthermore, to prove that the PES prototype will be capable of long-term operation, the thermal performance of the circuit was studied. To this end, a thermal camera (FLIR E55) was employed to observe and record the temperatures of the submodule during an hour-long heating test – so that the temperatures could settle in steady-state. The results from this test are depicted in Fig. 7. As can be seen, the heatsink temperatures are at roughly 50 degrees Celsius, which corresponds well to the thermal simulations performed earlier within the work package. Please note that higher temperatures are observed on the inductor, which is not part of the MoReSiC system; it is only used to test the prototype. Overall, the thermal operation of the PES prototype is validated.

(a)



(b)

Figure 7. Thermal tests of the ANPC leg– (a) exemplary thermal image from the camera, (b) temperatures of the system during an hour-long test at nominal operating conditions (1500 V DC, 6.5 kW).

4. Conclusions

The deliverable D2.2, “Laboratory prototype of the SiC-based power electronics submodule,” has been completed according to the schedule at the end of the 15th month of the project. The constructed Power Electronics Submodule (PES) has been successfully validated at the operating point with 1.5 kV DC voltage and the designed nominal power through a comprehensive experimental study. The switching performance of the module is satisfactory, with voltage overshoots at manageable levels, reaching roughly 10% for the best-case scenario with modulation PWM3. Furthermore, the power losses of the system were established, reaching below 200 W for the considered operating point, which corresponds well to earlier estimations performed during the design of the prototype (D2.1). Similarly, the thermal performance was also tested, reaching satisfactory temperatures at roughly 50 degrees Celsius, which is in accordance with the prior simulation study. All in all, the performed experimental tests successfully validated the design of the ANPC submodule as capable of operating in the required range of power, with low power losses, excellent thermal performance, and good switching performance. Thus, the power module could have been well applied as the core part of the power converters further to be built within the project.