Modularized, Reconfigurable and Bidirectional Charging Infrastructure for Electric Vehicles with Silicon Carbide Power Electronics (MoReSiC)

Deliverable D4.1 (Month 6)

Title: "The complete design of the AC/DC converter."

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Executive summary

The deliverable includes the complete design of the 20 kVA AC/DC converter, which is an input stage to the EV charging station. It was performed by the team from Warsaw University of Technology with support from Markel in terms of mechanical design. After the analysis, the Active Neutral Point Clamped topology was selected, and the submodule developed in the frame of WP2 was a base of the designed inverter. At first, a series of simulations were performed to choose the configuration with six SiC MOSFETs as a switches, then different PWM strategies were validated using PLECS software. Then the power section was designed with the support of Markel experience in CAD-based mechanical design. Finally, the control algorithm for the grid-connected three-level ANPC was developed and suitable DSP-based controller was designed.

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1. Multilevel topology selection

The research in WP4 started with the selection of the AC-DC topology. The main function of the inverter is to combine the three-phase grid (3x400V) with the three-wire DC-link (+750/0/-750V), also considering bidirectional power transfer. Simultaneously, the inverter should be designed based on SiC power devices. Therefore, based on the available state-of-the-art SiC MOSFETs and most common blocking voltage levels, it was decided to use a three-level AC-DC bidirectional converter, which allows using power semiconductors with 1.2 kV ratings.

Fig. 1 shows the three-level bidirectional AC/DC converter structure with a three-pole DC link. Based on a literature review, four different types of three-level bidirectional converters were selected from tens of existing topologies, as the most prominent ones, either through their exquisite performance or technology maturity. The phase legs of the considered topologies are shown in Fig. 2. In all the presented AC/DC structures, the maximum voltages on power semiconductors are reduced because of the three-level structure.

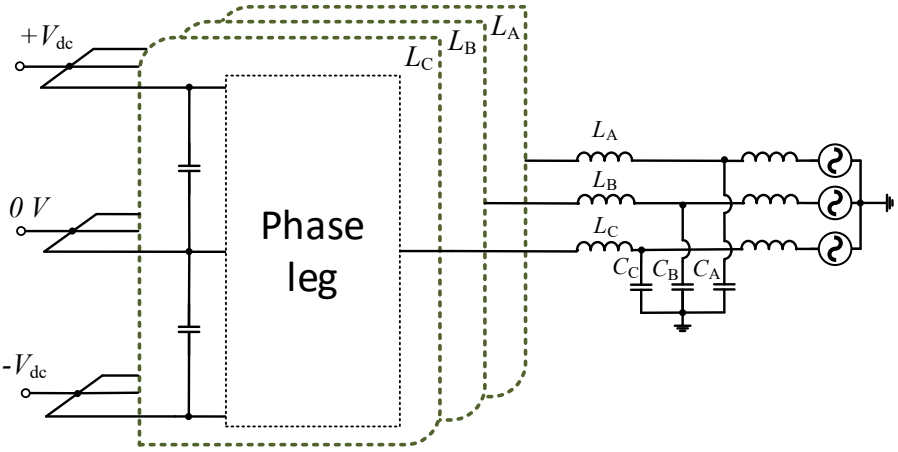


Fig. 1 Three-level bidirectional AC/DC converter

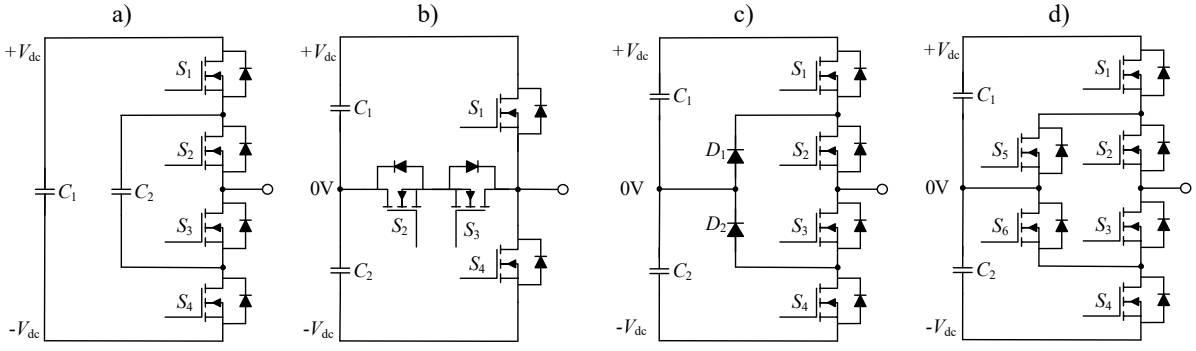


Fig. 2 Different types of three-level bidirectional AC/DC phase leg: a) Flying Capacitor, b) T-type, c) NPC, d) ANPC

In the AC/DC Flying Capacitor Converter (FCC), shown in Fig. 2a, four active switches are used, which is beneficial both in terms of cost, as well as overall efficiency. Additionally, only a single capacitor can be used in the DC-link. However, in this case, it renders this topology

unusable in the scope of the considered system, as the converter phase legs cannot be connected to the 0 V potential in the three-wire DC-link structure, which in consequence, makes it impossible to balance the voltage between the DC-link capacitors.

In the T-type converter, also only four power active switches are employed, exhibiting similar advantages as in the flying capacitor topology. Furthermore, this structure also shows very high possible efficiencies, as well as high quality of the grid current. Besides, the converter is suitable for a 3-pole DC-link, and allows for balancing the voltages between the DC-link capacitors. However, in this converter, the type of connection between the power transistor prevents to use three-level H-bridge structure, which is required to design a universal power submodule, common to all converters in the MoReSiC system, establishing the modular structure for each converter in the charging station (WP2).

Fig. 2c depicts a Neutral Point Clamped Converter (NPC), well known since 1981. While it also employs also four transistors, two additional power semiconductor devices, in the form of power diodes, have to be also used. Applying this topology, it is possible to connect to the common DC-link, as well as to balance the voltages between the DC-link capacitors and transistors are connected in H-bridge three-level structure, thus the NPC converter could be employed in the MoReSiC system.

However, another well-known topology, similar to Neutral Point Clamped Converter, shown in Fig. 2d can also be considered. Here, replacing the power diodes D_1 and D_2 (in the NPC topology) with transistors S_5 and S_6 (ANPC) allows for reducing the voltage spikes and oscillations on the transistors, which helps to establish a balance between the maximum v_{DS} voltages and achieving higher efficiency than in the NPC converter through turning on all middle transistors (S_2, S_3, S_5, S_6) during the zero state.
A comparison of all discussed topologies is shown in Tab. 1.

Tab. 1 Comparison of different three-level AC/DC converters

	Flying Capacitor	T-Type	Neutral Point Clamped	Active Neutral Point Clamped
Balance between $+V_{dc}$ and $-V_{dc}$ voltages	NO	YES	YES	YES
H-bridge structure	YES	NO	YES	YES
Active switches per leg	4	4	4	6
Diodes per leg	0	0	2	0
Power losses	Low	Low	Medium	Low

Based on the properties of the different three-level AC/DC converters described above and shown in Tab. 1, the ANPC converter was selected as the most appropriate for the AC/DC grid converter in the MoReSiC system. Even though its cost is quite high, since 6 active switches are used per leg, the many benefits of improved efficiency, lowered voltage overshoots, high flexibility in terms of the control, as well as satisfactory grid power quality make this topology the most prominent in the considered application.

2. Simulations oriented on efficiency

The next stage of the work was the simulation-based efficiency-oriented design of the 20 kVA AC-DC converter. The simulation study was conducted in PLECS software dedicated to power electronics simulations. A study on efficiency, thermal considerations, different modulation types, and closed-loop control using abc-to-dq Clarke-Park transformation was carried out. The research was conducted under sinusoidal PWM (SPWM) modulation with third harmonic zero-sequence voltage injection (ZSVI) at 1.5 kV DC-link, 3x400 V line-to-line input grid voltage, nominal power up to 20 kVA and for switching frequency 64 kHz. In the ANPC converter, it is possible to combine IGBTs and MOSFETs in one phase leg. Fig. 3 shows three different types of transistor connection in the ANPC converter: a) two SiC MOSFETs and four IGBTs, b) four SiC MOSFETs and two IGBTs, and c) six SiC MOSFETs without IGBTs. In such converters, MOSFETs are switching with high frequency, while IGBTs operate with fundamental frequency (50 Hz), which nearly fully eliminates IGBTs power switching losses.

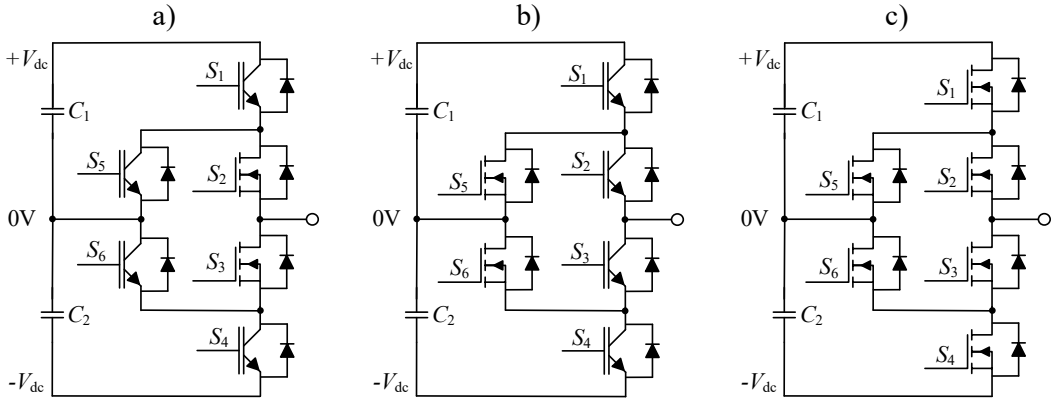


Fig. 3 ANPC converter: a) 2 SiC, b) 4 SiC, c) All-SiC

To check the efficiency of the energy conversion in different ANPC converters, simulation research was conducted. Each simulation model differs in the used transistors and the modulator, which provides the control signal to the transistors. The different modulation strategies analyzed for the ANPC converter are shown in Fig. 4.

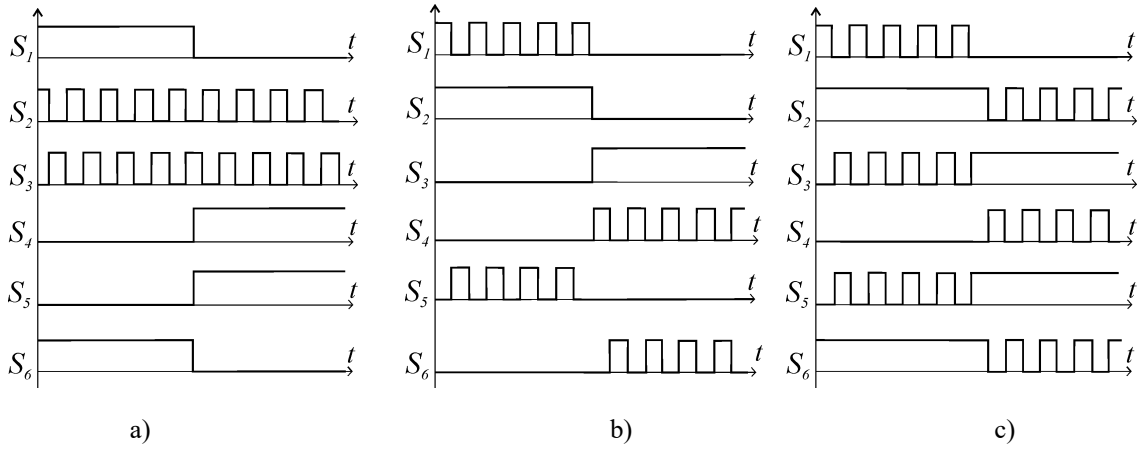


Fig.4 Different modulation strategies for the ANPC converters (a) 2-SiC, (b) 4-SiC, (c) All-SiC

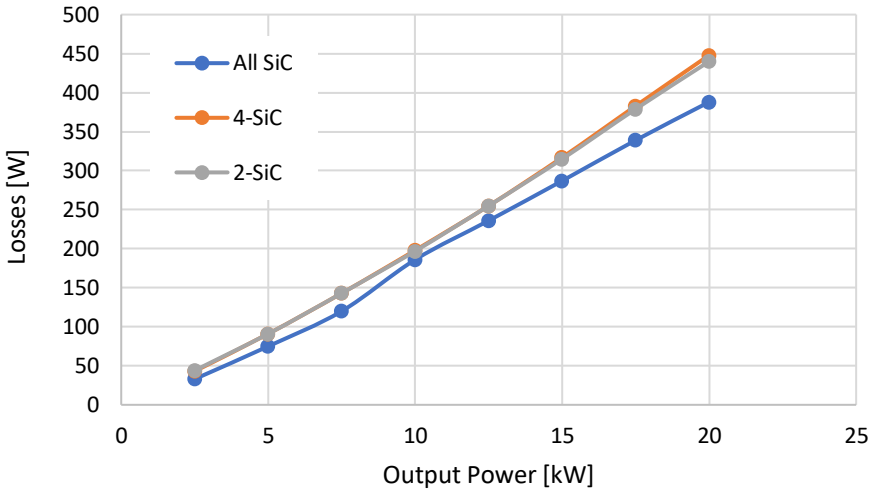


Fig. 5 Transistors losses in different ANPC converter

The power losses in the ANPC transistors obtained by simulation are shown in Fig. 5 for different types of transistors in the ANPC converter. For this analysis comparing the three options, in the simulation tests, the model of IKY40N120CS6 transistor was employed as the IGBTs, while the model of C3M0032120K was used for the SiC MOSFETs.

The smallest power loss in the whole output power range is for the All-SiC converter and is around 388 W for 20 kW of output power. Regarding the considerations within WP2 on the modularity and employment of a universal submodule, and based on the analysis shown above, the All-SiC ANPC converter was selected for the MoReSiC system as a high-efficiency solution, which can be used in three-wire DC-link with H-bridge, the three-level structure of the transistors.

After the ANPC topology selection, the next simulation research was conducted to select specific SiC MOSFETs and estimate their power losses required for the design of the converter. Based on simulation results, rms (root-mean-square) currents in power SiC transistors have been established. With those currents and $R_{DS(on)}$ resistance, turn-on, and turn-off losses from the datasheet, the power losses of the power semiconductors were calculated for different types of MOSFETs. Fig. 6 shows the power losses in transistors in one phase leg consisting of six power SiC MOSFET for nominal output condition and 64 kHz switching frequency.

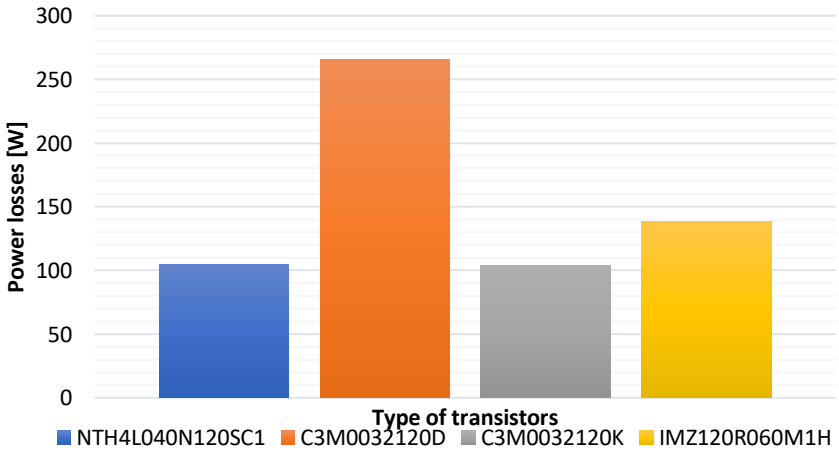


Fig. 6 Transistor power losses in one phase leg for a different type of transistor and nominal output conditions and 64 kHz switching frequency

Based on the simulation study and mathematical derivation, in agreement with WP2, NTH4L040N120SC1 SiC power transistors were selected. The estimated power losses in the power submodule with that type of transistor were similar to C3M0032120K and equal to 104 W. Simultaneously, the NTH4L040N120SC1 transistor was much cheaper than C3M0032120K. Power losses in other considering transistors were higher and equal 138 W for IMZ120R060M1H and 266 W for C3M0032120D.

3. The layout of the power section

Under task T4.3 (layout of the power section), the WUT team, in cooperation with the Markel team, designed the layout of the 20 kVA AC/DC converter prototype. As a base for the design, the parameters determined through the circuit simulations were assumed – see Table I. The power section consists of three power submodules constructed by Markel under WP2 (Fig. 7), a power board connecting submodules, and a precharging circuit. Fig. 8 shows the 3D model of the power bard, which also contains the measurement components, particularly the current transducers and voltage dividers, relays, and sockets for the gate drivers mounted from the top. Moreover, the suitable control board (described more thoroughly in section 6) was also designed to be mounted on the top of the power section and gate drivers (Fig. 9). The converter was to be enclosed in the rack 3U case (133 mm x 428 mm x 450 mm), which corresponds to a volume of 25,6 dm^3. All the elements of the system have been designed with due care to reduce the negative effects of parasitic inductances, keep minimum distances between components, and minimalize the dimensions of the whole system. All PCBs were constructed using Autodesk Eagle software.

Tab. I Basic parameters of the 20 kVA AC/DC converter

Line-to-line grid voltages v_a, v_b, v_c	3 x 400 V
DC-link voltage $V_{dc1} + V_{dc2}$	1.5 kV
Switching frequency	62.5 kHz
Filter inductances L_A, L_B, L_C	330 µH
Filter capacitances C_A, C_B, C_C	4.7 µF
DC-link capacitances	6 x 60 µF
Power SiC transistors	18 x NTH4L040N120SC1
Number of submodules (WP2)	3

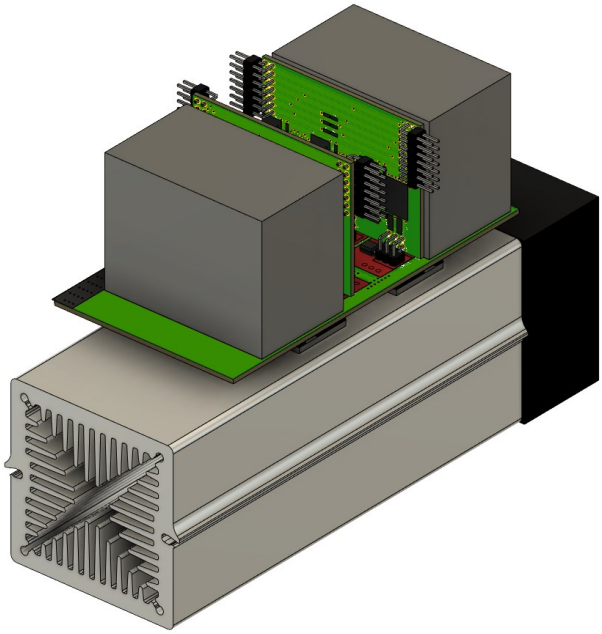


Fig. 7 3D model of the power submodule.

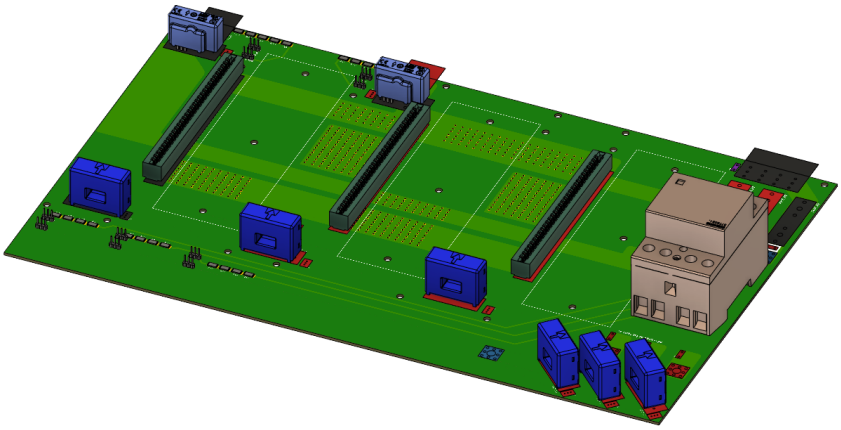


Fig. 8 3D model of the power board.

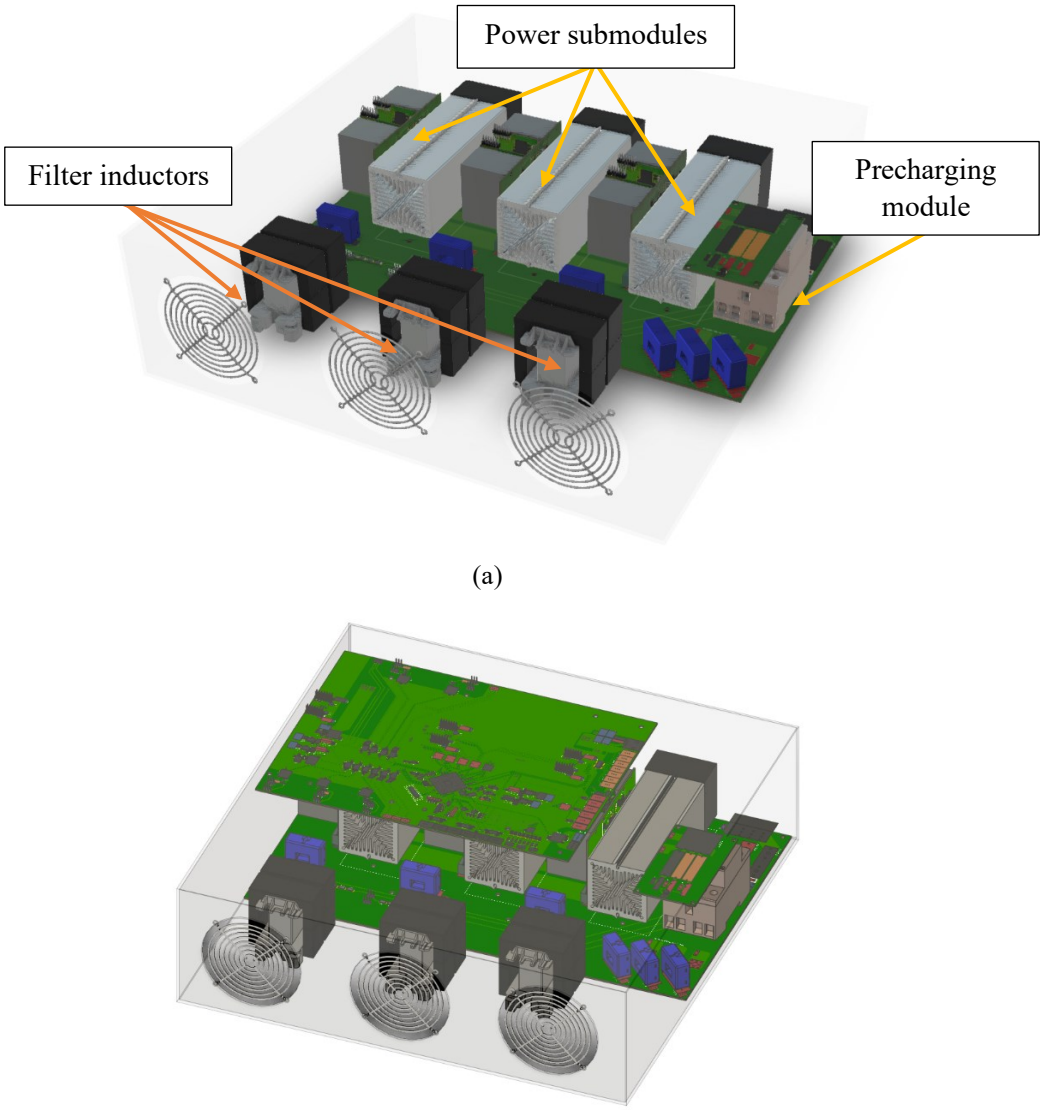
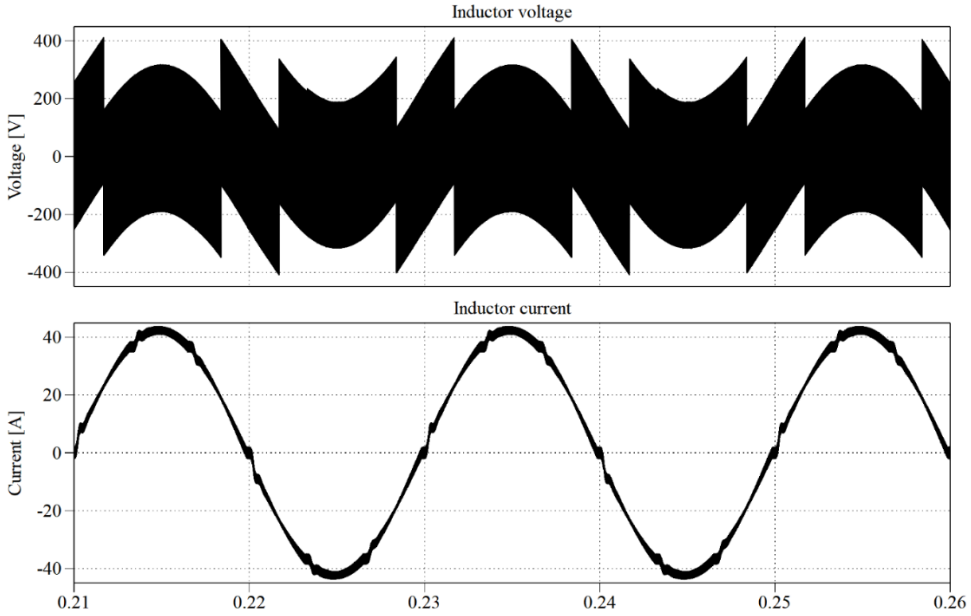


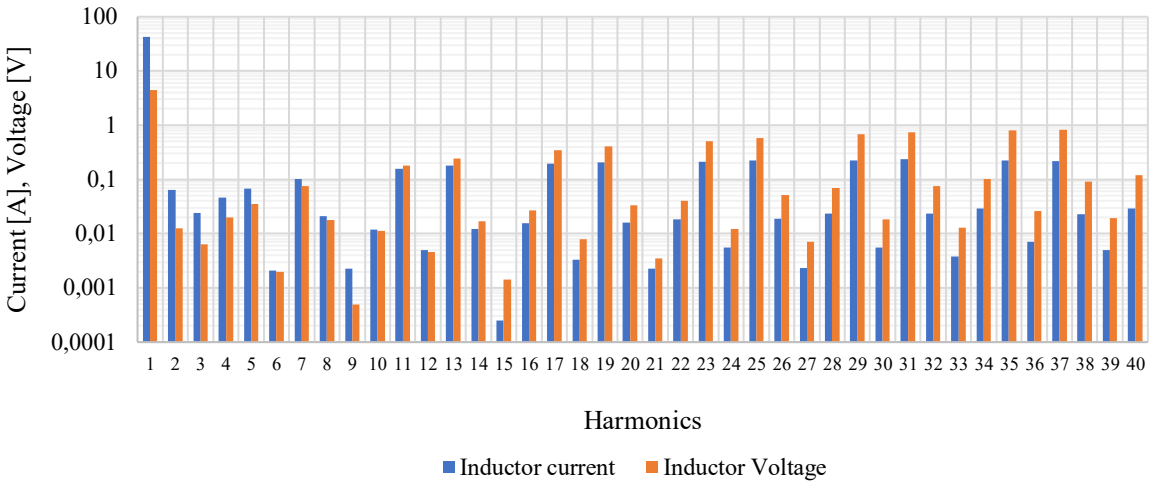
Fig. 9 The 3D model of the 20 kVA AC/DC converter without (a) and with (b) the control board.

4. Magnetic components

Under task T4.4 (Design of the magnetic components), the WUT team focused on the design of the input filter inductors. Based on the simulation results and theoretical analysis, and assuming around 10% filter inductor current ripple at its maximum value (around 42A), 330 µH inductors were chosen. Fig. 10 shows the input filter voltage and current for 330 µH inductors, 20 µH of grid inductance, 4.7 µF grid filter capacitance, and nominal conditions of the output and input parameters (1.5 kV DC link, 20 kW of output power, 3x400 VAC of input grid voltage) and closed-loop control described in the next section.



a) Voltage and current on input filter inductor



b) Harmonics of voltage and current of the input inductor

Fig. 10 Voltage and current of the input filter inductor

An inductance 330 µH allowed to obtain current THD of around 3.2%, which is an acceptable value within the requirements of the system (<5%). After an initial market analysis, it was concluded that an external supplier with off-the-shelf solutions could deliver the inductors capable of operating under simulated conditions. The commercial solution in the form of power inductors from Feryster was chosen, as it provided satisfactory parameters. To be more thorough, the employed powder cores EMS-0653327-040, were used in two pairs for reduced maximum flux density B and number of turns, which leads to lower copper weight, and lower power losses. Furthermore, according to the data provided by the manufacturer, the inductance loss is at roughly 57% of the nominal value for the nominal current of 42 A, which is an acceptable value for the system. Moreover, used Litz wires additionally help to limit the power losses of the inductors. All in all, based on the analysis using the datasheet of the power inductors, DEMS-65X54/0,33/31 model was used in the design.

5. *Control algorithm for bidirectional operation*

Under task T4.5 (Control algorithm for bidirectional operation), the team focused on designing the control algorithm of the constructed ANPC converter for bidirectional operation. Fig. 11 shows a schematic of the ANPC control algorithm.

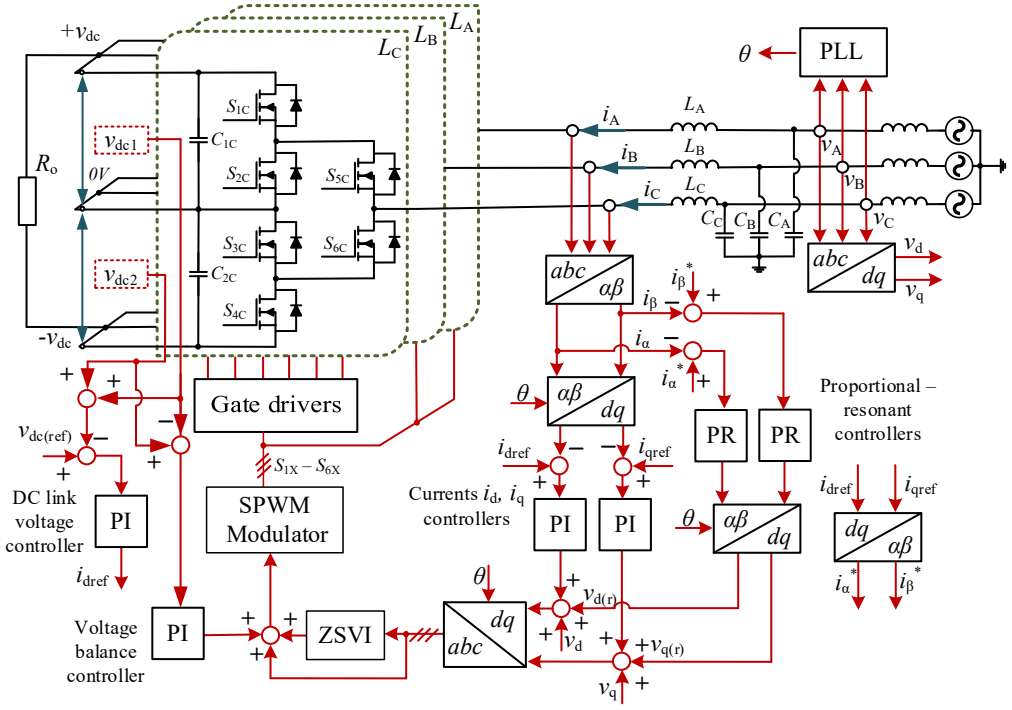
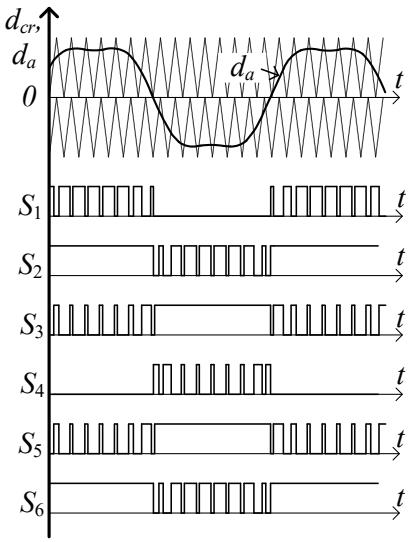


Fig. 11 Control strategy of the ANPC converter

The algorithm is based on the Clarke-Park transformations, which allow using PI controllers to control the grid current in the rotating reference frame domain (*dq*). Grid current level in *dq* domain is determined by the DC-link voltage controller through stabilized $v_{dc1} + v_{dc2}$ voltage. The quality of the grid currents is improved by using proportional-resonant (PR) controllers in the stationary reference frame domain (*αβ*). In the algorithm, the PR controllers for 5th, 7th, 11^{th,} and 13th harmonic of the fundamental frequency are used. The balance between DC link voltages v_{dc1} and v_{dc2} is assured by using an additional voltage balance controller based on the difference from the measured values of v_{dc1} and v_{dc2}. To reduce the conduction losses in power transistors, and to improve the balance on DC-link voltage capacitors, the zero-sequence-voltage-injection (ZSVI) signal is added to the sinusoidal modulation signal. In the last step, SPWM+ZSVI modulation signal is converted to the transistor control signal in the SPWM modulator block. Exemplary modulation, along with the gate driver signals, are depicted in Fig. 12. The basic transistor switching states for one leg of the ANPC converter are also included.



a)

switch \ state	$-V_{dc}$	0 V	$+V_{dc}$
S_1	0	0	1
S_2	0	1	1
S_3	1	1	0
S_4	1	0	0
S_5	1	1	0
S_6	0	1	1

b)

Fig. 12 ZSVI+PWM modulation signal and gate driver signals (a), and transistor switching states of one leg of the converter (b)

After the initial theoretical analysis and the selection of the proper topology and control for the grid converter, a thorough simulation study, including power loss estimation and a complete control system, was conducted. PLECS simulation environment from Plexim was employed, as it allows for easy simulation with direct possibilities to adapt the code for microcontroller use. The simulation model, apart from the basic static analysis, also regarded the system's dynamics, such as start-up or various changes in the power flow direction and levels. Furthermore, the parasitics expected in the real-life model were also included to mimic the actual operation of the converter as well as possible. Exemplary waveforms from the simulation with the grid converter operating at 20 kVA power and with 1500 V DC voltage in rectifier mode are shown in Fig. 13. The process of turning on the converter can be divided into six periods. At the beginning (t_1), the PWM signals are switched off, which means that the transistors are not operating. At the beginning of the period, t_1 precharging relay consisting of a three-phase diode rectifier with series-connected capacitors is turning on. The current flows through the precharging circuit to the DC link capacitor until $v_{dc1} + v_{dc2}$ voltage is roughly equal to the line-to-line grid voltage. Next, at the beginning of interval t_2, the AC relay is turning on, which connects the inverter directly to the grid. During the considered interval, the precharging circuit is switched off. In the next step (t_3), the converter starts to operate in the current mode, which enables only the current controller. Then (t_4), the voltage controller is turned on, and the voltage is increased through the ramp to the designed voltage ($v_{dc1} + v_{dc2}$ = 1.5 kV). At the beginning of the last interval (t_5), the DC relay is turned on, which connects the 112 ohmic resistors to the DC-link . In that particular example, when the nominal power is connected, the voltage drop equals about 10% of the nominal voltage.

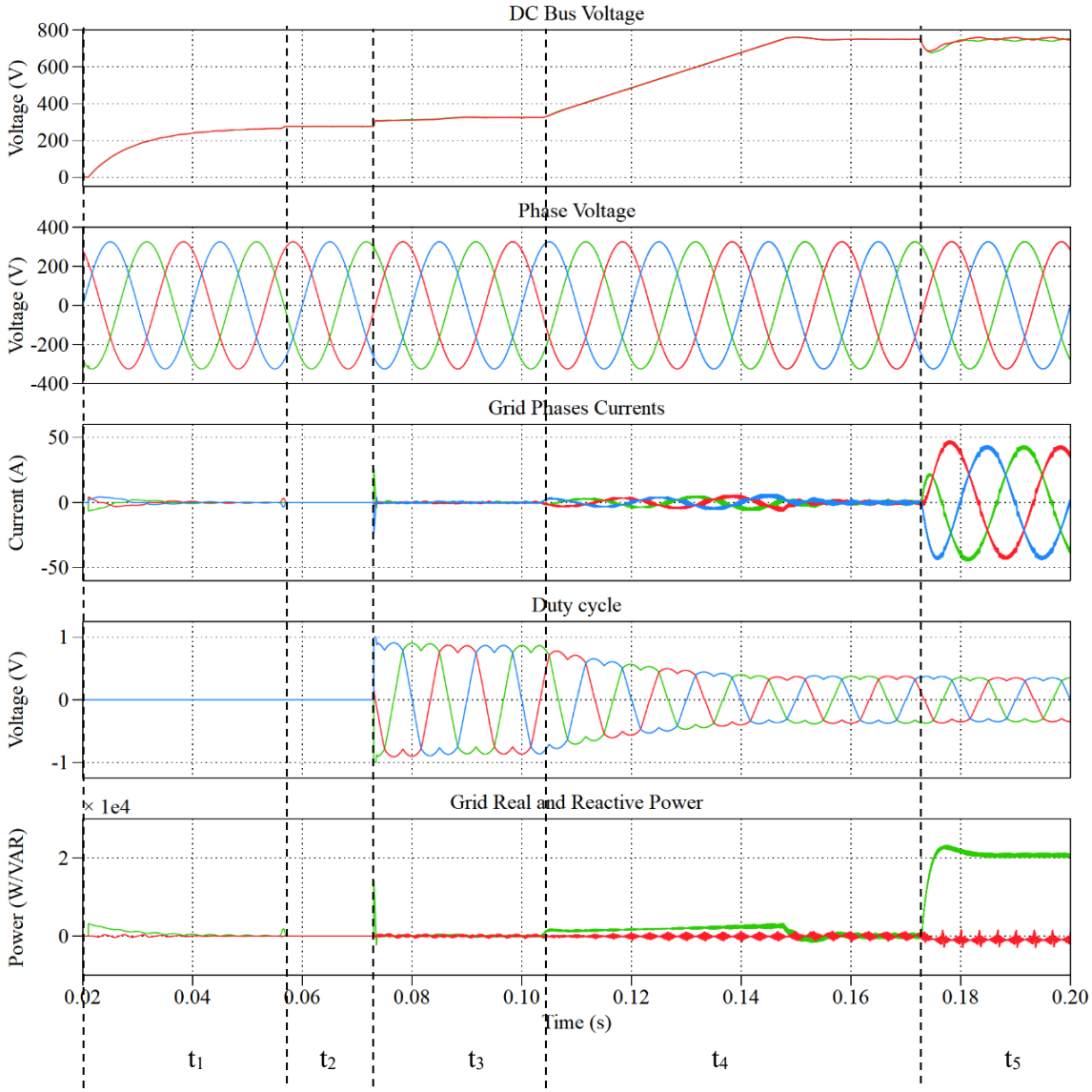


Fig. 13 Exemplary waveforms of the start-up process of the grid converter

6. *DSP-based controller*

In task T4.6 (DSP-based controller), a control board with DSP-based controller TMS320F28388D has been developed for project purposes. The model of the controller is depicted in Fig. 14. Currents are measured by using LEM current transducers, and voltages are measured with voltage dividers installed on the main powerboard (see Fig. 8). The control board also consists of conditioners to adjust the measured voltage signals to a voltage level suitable for DSP's analog-to-digital converter. The circuit also includes relays control outputs to connect the converter to the grid, common DC-link, or enable the precharging circuit. Moreover, the control board contains many other components such as logic voltage translators that adjust the DSP's output voltage to the input voltage of the gate drivers, outputs for controlling the cooling fans of the power submodules heatsinks, micro converters for supplying required power for control board components, relays and cooling fans. After the initial validation, the proposed

control algorithm described in section T4.5 was translated into C language using a software environment for the TMS320F28388D controller and was used to control the converter prototype.

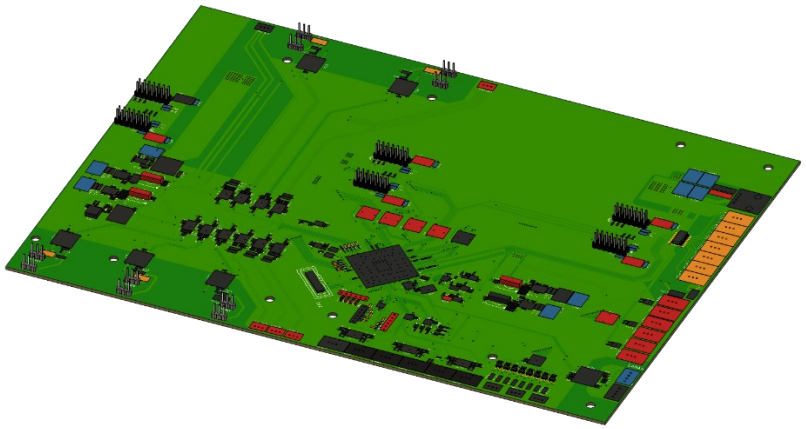


Fig. 14 Model of the control board.

7. Summary

Designing bidirectional AC/DC grid converters for a notable power of 20 kVA always is a challenging task. Especially so in the discussed system in the scope of the MoReSiC project, as additional constraints are necessitated, such as 3-pole DC-link connection, relatively high DC voltage of 1500 V, as well as the modular aspect directly associated with WP2, and the large variety of possible scenarios of power flow within the system. Nevertheless, the full design based on a theoretical and simulation study, starting from the topology selection, choosing the power devices and other parts, through establishing the proper control algorithm, to, finally, the PCB design of all the components of the converter. The provided design is sufficient to construct a prototype of the grid converter to be executed further in the project.