Modularized, Reconfigurable and Bidirectional Charging Infrastructure for Electric Vehicles with Silicon Carbide Power Electronics (MoReSiC)

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Title: "Design guidelines for the optimized, multiport and reconfigurable isolated DC/DC converter"

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Executive summary

This deliverable contains design guidelines in terms of electric circuit topology, electrical and thermal constraints, as well as power semiconductor requirements for the optimal design of the fundamental block for the multiport and reconfigurable DC/DC converter. The results presented in this document have been acquired through theoretical analysis, as well as electrical and thermal modelling and simulations. Four design aspects are presented here, namely fundamental circuit topology and multiport DC/DC converter configuration, electrical ratings and targeted efficiency, thermal ratings and power semiconductor devices.

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1. Circuit topology

It is found and recommended that the most suitable fundamental circuits for the multiport and reconfigurable isolated DC/DC converters are the full-bridge (FB) or the active neutral-point clamped (ANPC) circuits, as shown in Figs. 1 (d) and (e), respectively. These circuits can be combined for designing either one-to-one isolated DC/DC converters comprising a single primary and single secondary circuits or multiport counterparts. An example of a one-to-one isolated DC/DC converter employing an ANPC circuit in the input side and a FB circuit on the output stage that are coupled though a high-frequency transformer is depicted in Fig. 1(c). However, to increase the flexibility in terms of voltage and electric power supply or under input supply conditions imposing higher voltages, FB and ANPC circuits can be connected in series or in parallel in order to meet the design constraints.

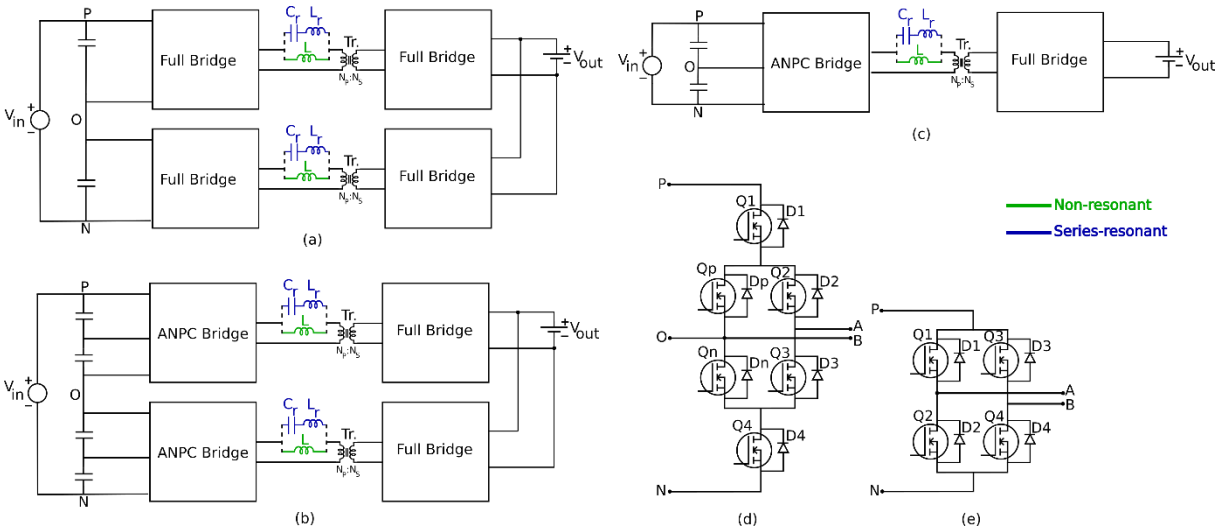

Fig. 1: Block diagrams of the evaluated topologies: (a) ISOP FB DAB, (b) ISOP ANPC DAB, (c) ANPC DAB, (d) ANPC bridge, and (e) Full bridge.

Assuming a DC bus having a nominal voltage of 1.5 kV and that the one-to-one configuration is rated at 10 kW, two recommended configurations of the multiport DC/DC converters are shown in Figs. 1(a) and (b). The first one (ISOP FB, Fig. 1(a)) consists of two series-connected FB circuits employing 1.2-kV class power devices on the input (i.e., primary) side in order to sustain the DC voltage of 1.5 kV. In particular, each of the two FB circuits blocks 750 V. For supplying the targeted voltage of 400 V to charge the electric vehicle (EV) and electric power that is a multiple of the rated power of the one-to-one configuration, the output (i.e., secondary) stage should be designed with parallel-connected FB circuits. The example shown in Fig. 1(a) contains two FB circuits on the output and thus, supplies 20 kW of power. However, by parallel connecting a higher number of FB circuits on the output, a higher power can be achieved (e.g., 3 FB circuits supply 30 kW etc.).

The second recommended configuration is shown in Fig. 1(b). In this multiport DC/DC isolated converter, the primary side contains two series-connected ANPC circuits employing 650-V class power devices. Each ANPC circuit must withstand half of the DC bus voltage of 1.5 kV, which also dictates the design choice of 650-V rated power semiconductors.

The two presented configurations can be either designed as regular and non-resonant dual-active bridge (DAB) converters or as resonant converters. The design difference is the need for an additional resonant circuit for the latter configuration, as shown with the blue colour in Figs. 1(a)-(c). Both the resonant configuration and the non-resonant system operates with single-phase shift modulation. In resonant configuration, the switching frequency is set higher than the resonant frequency to enable continuous current mode operation. The amount of power transfer is controlled using the phase-shift angle while the power flow direction is dependent on the polarity of phase shift. Only a small variation of the phase shift is needed to regulate the output from full load to almost no load In case of non-resonant configuration, a single inductor is required to ensure controllability of the power flow between the input and output stages of the DC/DC converter. The value of this inductor, L, should be calculated as:

$$L = N * V_{primary} * V_{secondary} * \frac{(D*(1-D))}{2*f_{sw}*P_{out}} \qquad (1)$$

Where, D is the phase-shift between primary and secondary bridges, assuming that single-phase shift modulation is used. The values considered for dc input voltage (V_{in}), DC output voltage (V_{out}), output power (P_{out}), switching frequency (f_{sw}), non-resonant/resonant inductance (L/L_r), resonant capacitance (Cr), and transformer turns ratio (N) are summarized in Table I.

Table I: Design parameters

DAB type	Non-resonant DAB	Series-resonant DAB
V_{in}	1500V	
V_{out}	400 V	
P_{out}	10 kW	
f_{sw}	100 kHz	
L/L_r	17µH – 70µH*	100 µH
C_r	-	28 nF
N	$V_{primary}/V_{secondary}$	

$V_{primary}$ - peak transformer primary voltage
$V_{secondary}$ - peak transformer secondary voltage
*Calculated using Eqn.1 depending on topology

2. Power semiconductors

The choice of power semiconductor devices must be made based on the anticipated optimal performance of the specific configuration. For the investigated DC/DC multiport converters, Silicon Carbide (SiC) metal-oxide semiconductor field-effect transistors (MOSFETs) have been chosen. The specific voltage ratings should be chosen based on the DC bus voltage constraint (in this case 1.5 kV). On the other hand, the current ratings should be chosen by considering the electric power processed by each fundamental circuit, as well as the thermal effect (i.e., temperature) and the utilised cooling system under normal operation.

Table II summarizes the chosen SiC power devices for achieving optimal operation of the presented multiport DC/DC converter configurations above.

Table II: MOSFET model information and parameters

Topology	MOSFET used in primary bridge	MOSFET used in secondary bridge
ISOP FB DAB	NTH4L040N120SC1[1]	C3M0015065K[2]
ISOP ANPC DAB	IMZA65R039M1HXKSA1[3]	C3M0015065K[2]
ANPC DAB	NTH4L040N120SC1[1]	C3M0015065K[2]

[1]1200V, 40mΩ, 58A SiC MOSFET from ON semiconductor
[2]650V, 15mΩ,120A SiC MOSFET from CREE
[3]650V, 39mΩ, 50A SiC MOSFET from Infineon

The optimal design for the multiport DC/DC converter should be based on the optimal choice of the voltage-current rating of the employed power semiconductors. Such a choice will impact the overall cost and performance of the system. Table III shows the required volt-ampere ratings for each of the three presented configurations, as well as their normalized cost.

TABLE III: Performance metrics of SiC MOSFETs

Topology	Volt-Ampere rating of MOSFETs (kVA)			Normalized total cost of MOSFETs*
ISOP FB DAB	Primary bridge	Secondary bridge	Total	
	556.8 (8 * 1200V * 58A)	624 (8 * 650V * 120A)	1180.8	2.34
ISOP ANPC DAB	390 (12 * 650V * 50A)	624 (8 * 650V * 120A)	1014	2.32
ANPC DAB	417.6 (6 * 1200V * 58A)	312 (4 * 650V* 120A)	729.6	1.44

*Cost normalized per 200 USD

3. Efficiency and Loss distribution – Simulation study

Fig. 2 presents the efficiency comparison and Fig. 3 illustrates a comparison of MOSFET loss distribution based on simulations, for the six considered topologies, at a power level of 10kW. It can be inferred that the series-resonant DAB configurations outperform the non-resonant variants. One possible reason for the better efficiency of SR variants is due to the operation of SiC MOSFETs near soft switching region in both primary and secondary bridges. This fact is reflected in the MOSFET loss distribution, where the switching losses in both primary and secondary bridges of the SR DABs (i.e., iv, v and vi in Fig. 3) are far lower compared to the

non-resonant DABs. An additional reason is the sinusoidal shape of the transformer currents in the SR DABs, which results in lower RMS currents and in turn lower conduction losses. This can be observed in Fig. 3, where the conduction losses of the SR DABs are lower in both primary and secondary bridges compared to the respective non-resonant variants.

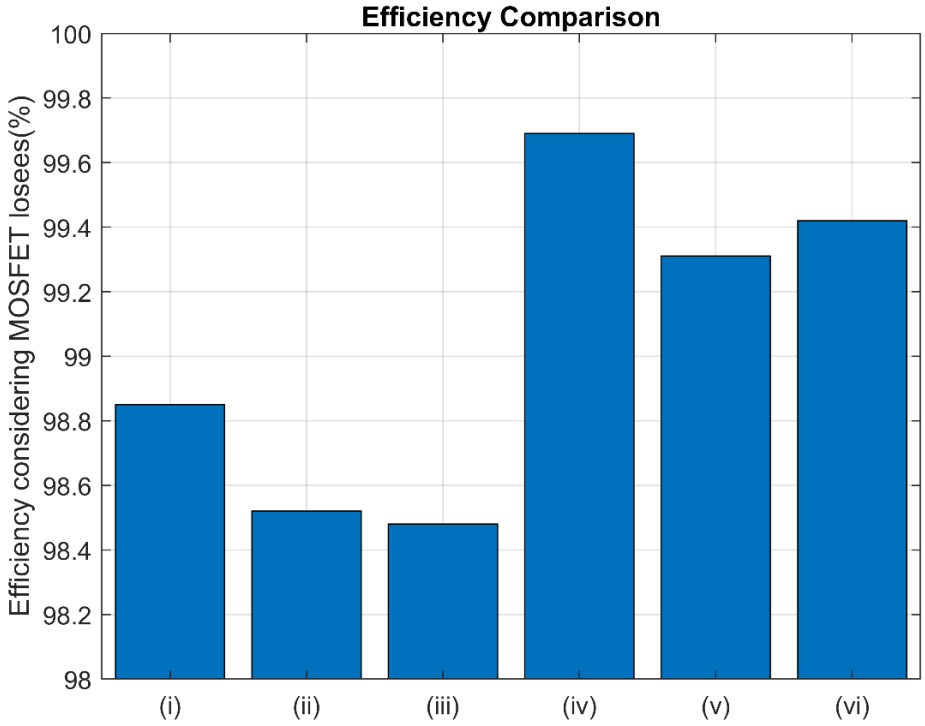

Fig. 2: Comparison of efficiency considering only the MOSFET losses based on simulations.

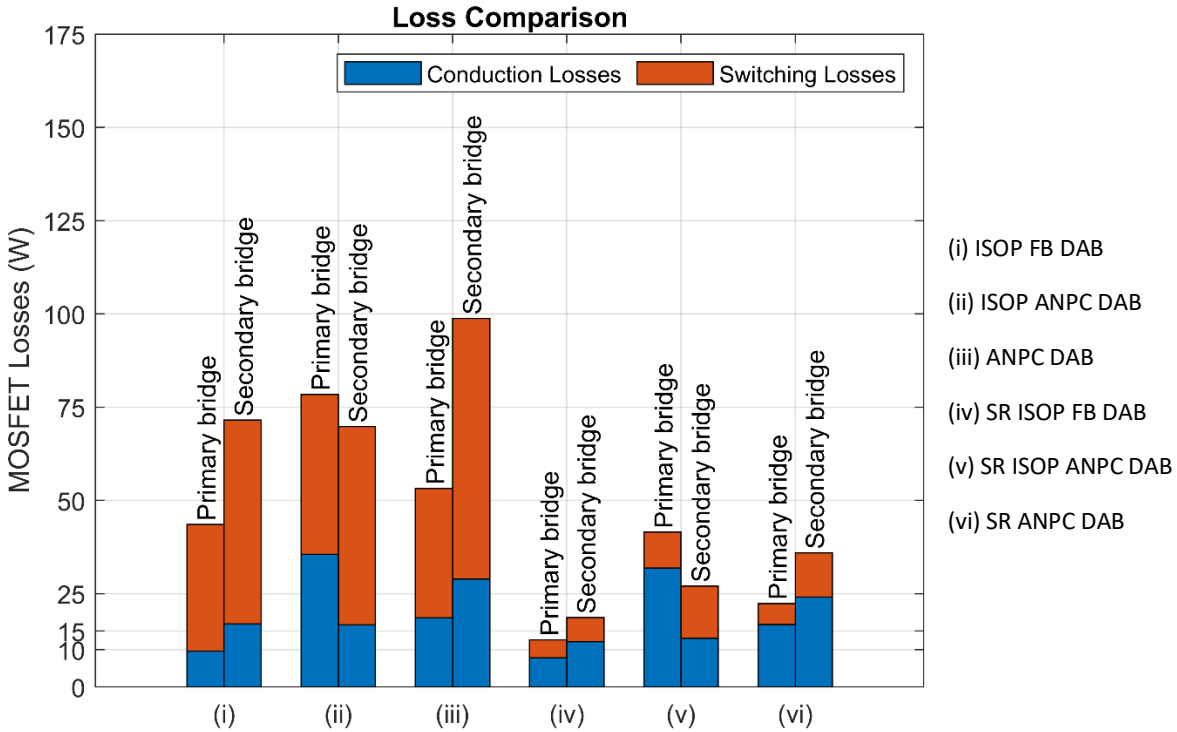

Fig. 3: Comparison of MOSFET loss distribution based on simulations.

Among ISOP FB DAB and ISOP ANPC DAB configurations, considering both non-resonant and SR variants, the main difference is the higher conduction losses in the primary bridge for the ISOP ANPC DAB as seen in Figs. 3 (ii) and (v). The reason for this is that ISOP ANPC DABs carry almost double the current in the primary bridge compared to ISOP FB DABs for the same power transferred, as only half of the input voltage is reflected on the transformer primary. The higher secondary bridge current (almost double) in non-resonant ANPC DAB compared to the ISOP topologies causes higher switching losses, since the MOSFET switching energy is dependent on drain current. This can be observed in Fig. 3 (iii).

4. Electrical ratings

It is recommended to set the power rating of each fundamental module at 10 kW, in order to reduce the design complexity and to utilise discrete power semiconductor devices. These are encapsulation technology that accommodates a single power semiconductor device, namely die. This practise enables the design of power circuit layouts having reduced parasitic inductance that impacts the fast-switching capability of SiC power devices. Thus, achieving shorter switching times, switching frequencies as high as 100 kHz can be used in the proposed configurations reducing the size of critical converter's components, such as magnetics.

5. Thermal ratings

The maximum die temperature should be set at 100°C. The reason for this is the positive temperature coefficient for the on-state resistance of the SiC MOSFETs, contributing to higher conduction power losses and also the need for more sophisticated cooling system designs.

6. Conclusions

Six different configurations of the IBDC DAB topology have been evaluated for a 10-kW EV charging application. The topologies were selected considering the bipolar (three-wire) nature of input DC bus, two-terminal nature of EV battery load, flexibility of voltage as well as power scalability. The spider plot in Fig. 4 summarizes the evaluation of the considered topologies based on the performance metrics discussed above. The series-resonant topologies exhibit higher efficiencies compared to their non-resonant variants, which can be attributed to their significantly lower switching losses. The FB topologies exhibit lower conduction losses compared to the ANPC topologies. In terms of VA ratings and normalized cost of SiC MOSFETs, the ANPC DAB topology has a clear advantage compared to the ISOP FB and ISOP ANPC DAB configurations. The SR ANPC DAB topology combines the advantages of both the series-resonant configuration (i.e., lower switching losses and higher efficiency) and the ANPC topology (i.e., lower VA ratings and normalized cost of SiC MOSFETs). This makes it the best design choice for the evaluated application, considering all performance metrics.

In terms of additional passive component required, sensitivity of the circuit performance in the control scheme and control complexity the non-resonant DABs have an advantage over the SR DABs. However, SR DABs have a higher number of soft-switched (zero voltage and zero current switching) MOSFETs and near sinusoidal transformer currents, which result in lower switching and conduction losses. These positive performance impact factors of SR DABs outweigh their challenges for the considered application and operating conditions. In terms of efficiency and SiC MOSFET losses, the series-resonant variants outperform the non-resonant DABs with the SR ISOP FB DAB exhibiting the best performance. When the normalized cost and the VA ratings of SiC MOSFETs are considered, the ANPC DAB configuration seems to

be the most promising one. Considering a fair trade-off between efficiency, loss distribution, VA ratings and the normalized cost, the SR ANPC DAB exhibits the best performance for this application.

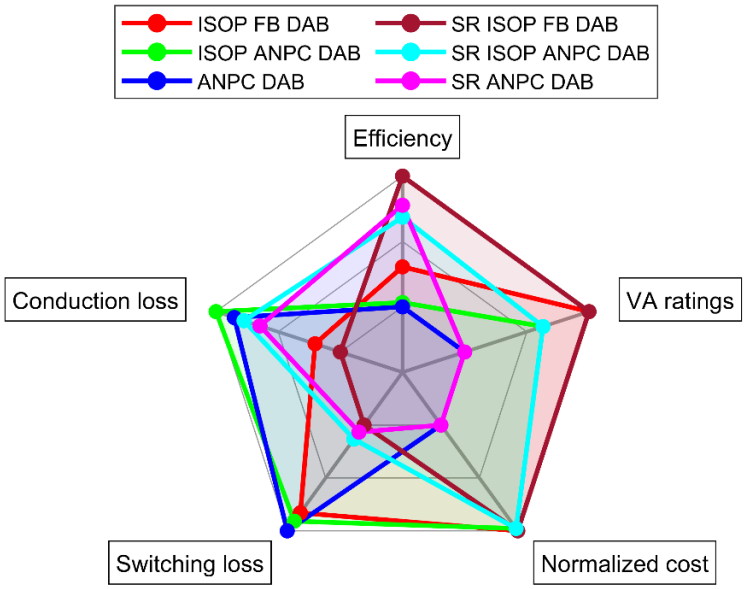

Fig. 4: Comparison of the evaluated topologies based on all the chosen performance metrics.