Modularized, Reconfigurable and Bidirectional Charging Infrastructure for Electric Vehicles with Silicon Carbide Power Electronics (MoReSiC)

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Title: "The layout of the power electronics submodule enabling easy adaptation to the needs of AC-DC and DC-DC converters"

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Executive summary

This deliverable concerns the process of designing a Power Electronics Submodule (PES) in accordance with the initial assumption of the universality of the solution and applicability for all converters constructed within the scope of MoReSiC project. The document presents technical requirements for PES provided by all project participants, selection of individual active and passive components taking into account their nominal parameters (currents, voltages, power losses, parasitic inductances), mechanical and electrical design, power loss calculations, and thermal simulations. Finally, the PES layout design using 3D CAD software was presented. Satisfactory thermal properties, compact design, and assumed universality of the Power Electronics Submodule were achieved.

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1. Preliminary technical requirements

One of the main tasks of the WP2 stage was to develop a Power Electronics Submodule (PES), the layout of which will allow for easy adaptation to all the AC-DC and DC-DC converters. Mainly for this reason, especially in the initial phase of work, the cooperation of all MoReSiC participants was required. The universality of PES required establishing a closed set of requirements that would allow for the free design of all converters. The main assumptions for the module have been established as follows:

- operation with a symmetrical, 3-pole DC network +/- 750 V

- rated power of PES at 10 kW

- single leg topology as the most versatile solution

- minimization of parasitic inductances to obtain the operating frequency up to 100 kHz

- SiC MOSFET elements adaptation to reduce power losses

- compact design to minimize electromagnetic interference

- easy installation and service (PES as an indivisible element for RACK 19' standard housing)

- high reliability and lifetime estimated at a minimum of 10 years of failure-free operation

- a set of protection functionalities against hardware damage

All noted assumptions were taken into account during the design process.

2. Topology and component selection

The MoReSiC project assumes the use of a symmetrical, 3-pole DC voltage network as an infrastructure for charging electric vehicles. The project also assumes the possibility of using high-voltage energy storage. In the proposed network structure, the converters can operate with the DC-Link voltage in the range of 750 V or 1500 V. Taking into account the universality of the module, the symmetry of the proposed power supply network, the parameters and availability of SiC MOSFET transistors, a three-level topology was chosen with 1200 V power semiconductors. Furthermore, the features of Active Neutral Point Clamped (ANPC) topology (e.g. improvement of the current THD ratio) determined the choice of this solution as the target for Power Electronics Submodule. Moreover, the design of PES also included the possibility to employ only 4 of the 6 power transistors so that a more conventional three-level topology could also be used.

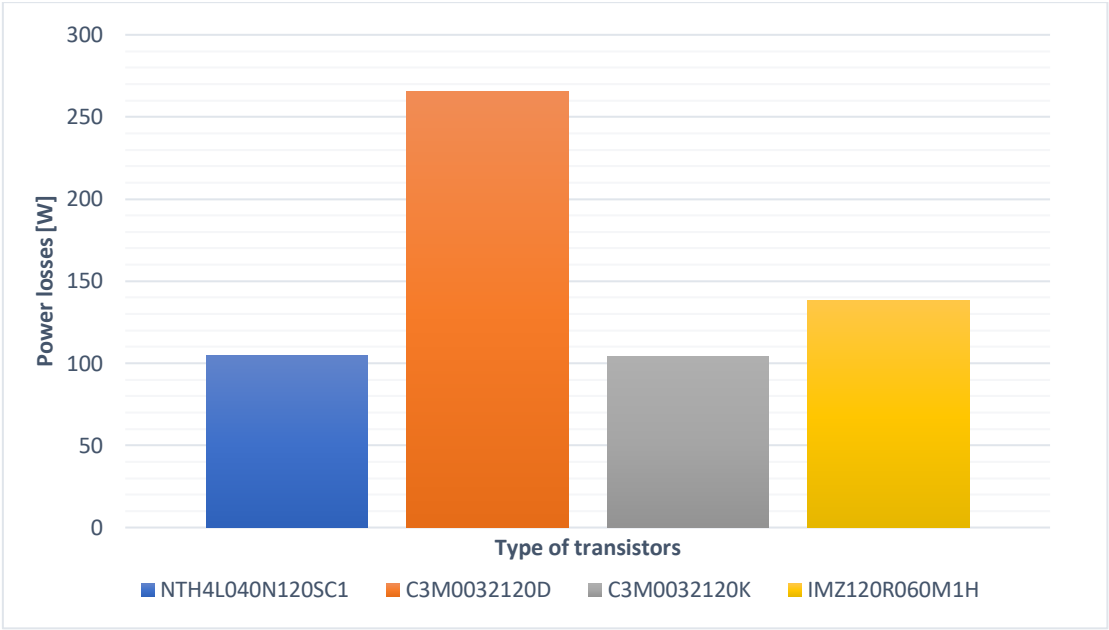
One of the most important processes during the development of the PES layout was the selection of the key components:

- Silicon Carbide MOSFET
- DC-Link Capacitor
- Heatsink

- Fan
- Power connector

The selection of a transistor for a power electronic device is a key decision that determines the level of efficiency, waveform quality, and electromagnetic compatibility. Taking into account the assumed PES power, possible DC-link voltages, and the selected topology, it was decided to select a SiC MOSFET with a voltage class of 1200 V, low switching energies, and To-247 housing with Kelvin Source Terminal for improved switching performance.

A comparative analysis of several off-the-shelf power devices was carried out. As a selection criterion, it was decided to choose an element with minimal power losses to maximize efficiency. Based on then-available SiC power transistors with good numbers according to their datasheets, state-of-the-art devices from three different manufacturers were chosen. Then, based on a combined theoretical and simulation-based analysis performed for the AC/DC grid converter and the non-isolated DC/DC converter for the battery energy storage system, a comparison of the power losses was prepared and is shown in Figure 1. Based on these results, it can be seen that in terms of efficiency, the NTH4L040N120SC1 transistor from onsemi showed the most prominent results and thus was chosen as the power transistor for the PES. Furthermore, the topology of the PES, along with averaged power losses for each of the transistors in the phase leg, is depicted in Fig. 2.



a)

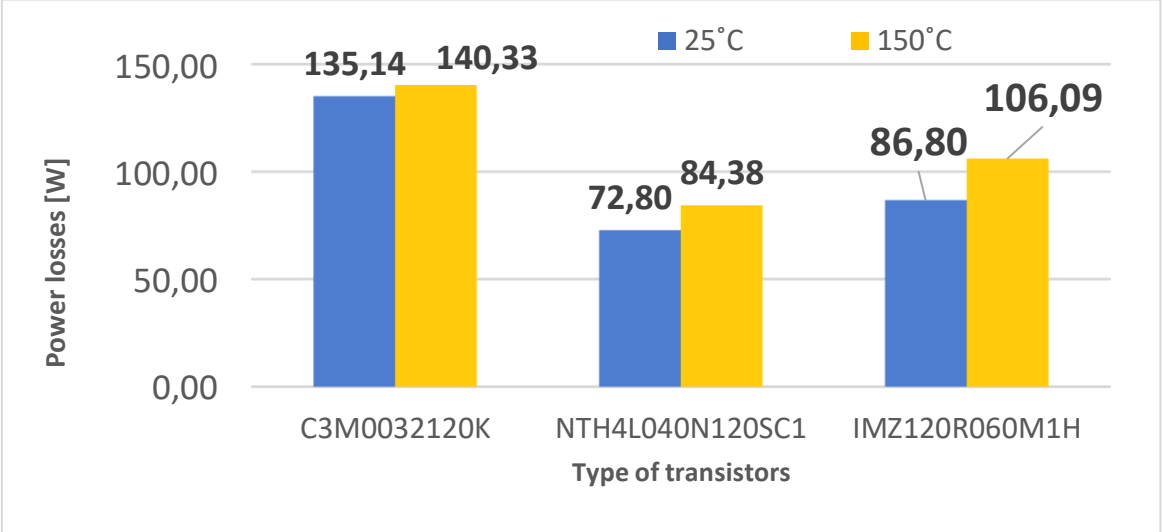


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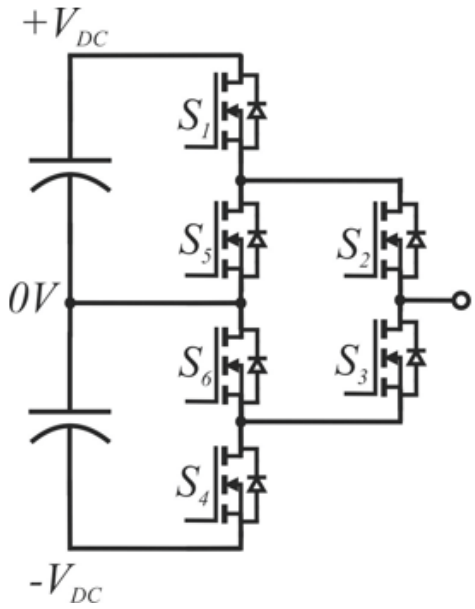
Figure 1. Power loss analysis performed for various state-of-the-art SiC power MOSFETs for the transistor selection process: results for the AC/DC converter (a), data from the study on the non-isolated DC/DC converter (b).



SiC MOSFET NTH4L040N120SC1 [@ 100 °C]	Power loss [W]	SUM [W]
S1	22	126 W
S2	25	
S3	25	
S4	22	
S5	16	
S6	16	

Figure 2. ANPC topology and averaged power loss of each transistor based on an analysis performed for the chosen transistor for the grid AC/DC converter and the non-isolated DC/DC converter.

An equally important element of the system as the power transistor is the DC-Link capacitor (especially in the case of applications with high switching frequencies). When selecting the component, apart from the capacitance and voltage, which are the obvious parameters of the capacitor, the focus was on the parasitic inductance and the mechanical design that allows for minimizing the external inductance of the commutation circuit. Finally, the capacitor C4AQIBW5600A3NJ was selected with a capacity of 60 µF, voltage 800 V, RMS current 27.5 A for 70°C, and parasitic inductance of 15 nH. The correctness of the electrical parameters selection has been confirmed by simulation tests and theoretical analysis.

Various air cooling systems were also considered. During the selection, attention was paid to the characteristics of thermal resistance, efficiency, and supply voltage of the fan, dimensions, and the possibility of easy assembling the selected transistors. A photo of the initially considered heat sinks is shown in Figure 3. Finally, the LAM 6-125 heat sink and the 618 J/2HHP fan were selected.

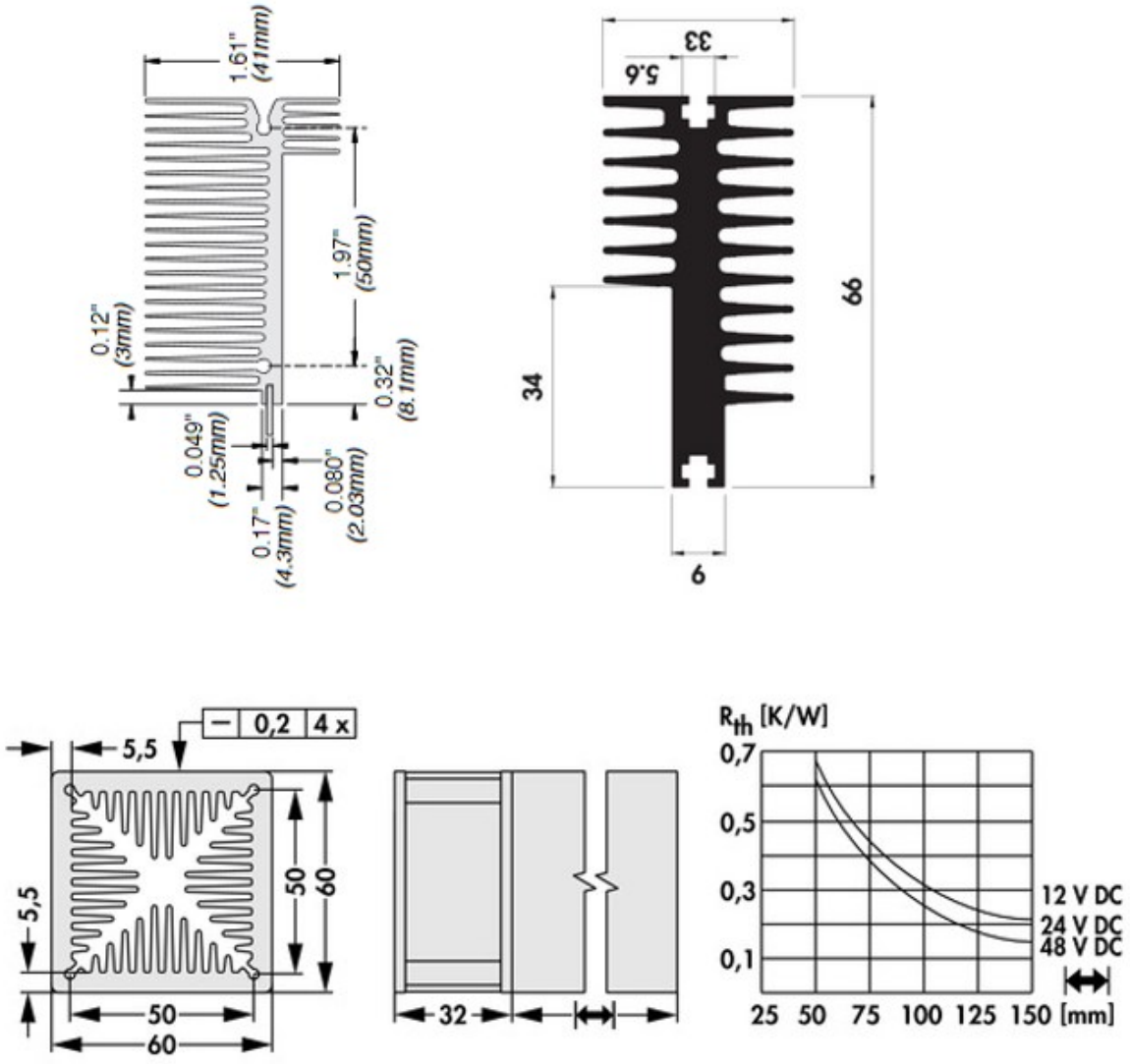


Figure 3. Different types of considered heat sinks

During the works, a power connector was also selected to connect the PES with the power boards of individual converters. The connector provides the ability to transfer power at the level of the assumed 10 kW and a robust mechanical structure. All key PES components are summarized in Table 1. It is worth noting that an additional criterion for the selection of all components was their availability and price at the time.

Table 1. A list of PES main components

Component	Description	Part number
Transistor	SiC MOSFET	NTH4L040N120SC1
Capacitor	DC-Link capacitor	C4AQIBW5600A3NJ
Connector	Power connector	305-060-520-201
Heatsink	Heatsink	LAM6-125
Fan	Fan	618 2HHP

3. PCB designs

The PES project includes 2 types of PCB: power PCB and gate driver PCB. The design of the power PCB is crucial from the point of view of all converter performance parameters. It must meet the thermal requirements and ensure the minimum parasitic inductance of the commutation circuit. In order to meet both requirements, the power board was made of 4 layers with 105 µm thick copper. Gold-plated PCB-type connections reduce the transition resistance and increase the service life of the PES. The design of the power board must also be compact. Minimizing the size not only helps to achieve low parasitic inductances but also reduces the emission of electromagnetic interference. The appearance of the power board (production version) is shown in Figure 4.

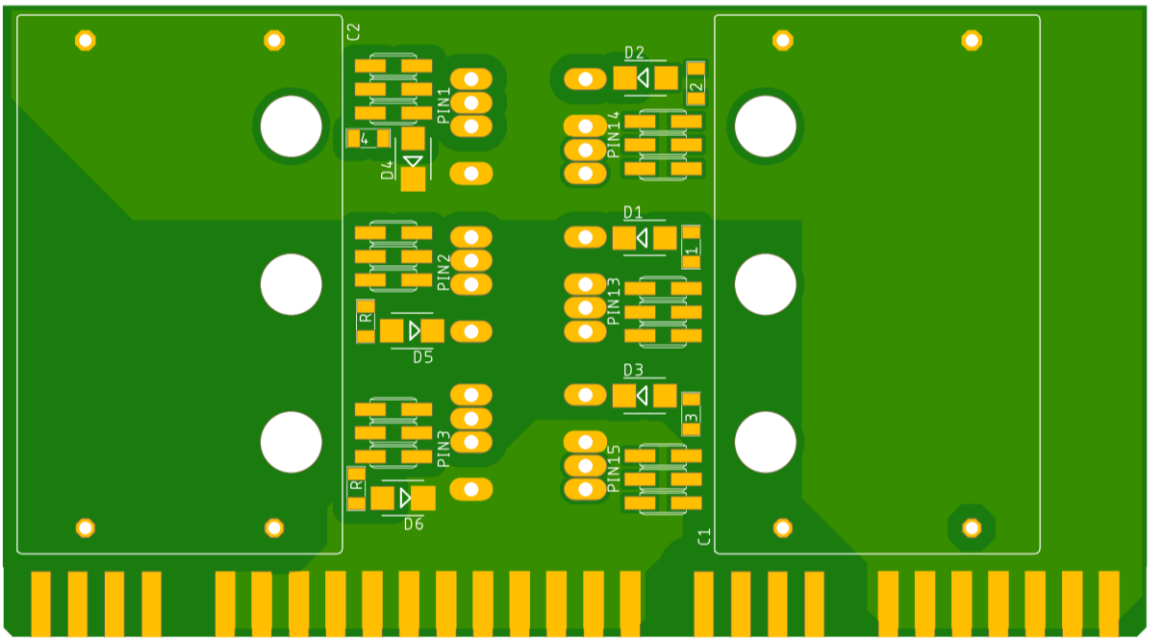


Figure 4. Power PCB

The gate driver is an essential element of any power converter. It fulfills two main functions. It provides appropriate electrical parameters for the gate circuit of the transistor, which results in its correct, low-loss switching process. On the other hand, the gate driver must provide galvanic separation between the control system and the power circuit. The main elements of the designed gate driver are a separated DC/DC converter with secondary voltages -5/20 V suitable for the SiC MOSFET transistor and an integrated optical driver ensuring separation at the level of 5 kVac (50 Hz, 60 s). The gate driver provides PES protection functions: short-circuit detection, undervoltage, and temperature protection. The PCB of the gate driver was designed in a 2-layer version with 35 µm thick copper. The pins have been adapted to the socket on the power board. The appearance of the gate driver PCB is shown in Figure 5.

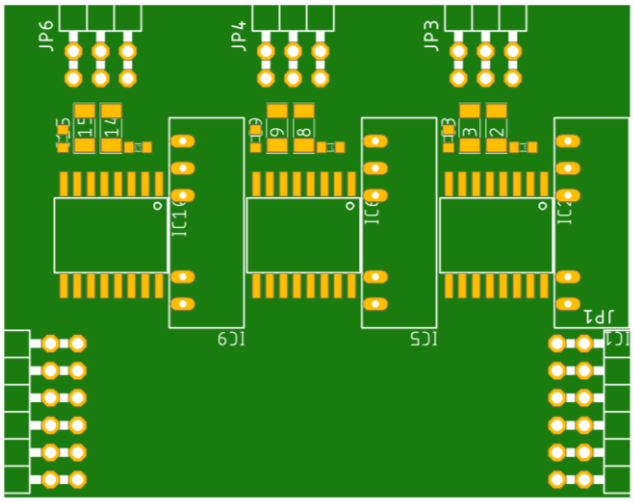


Figure 5. Gate driver PCB

For a compact design, one gate driver PCB has 3 independent, isolated channels supporting 3 gate drivers. The gate drivers are designed to be connected directly to the power PCB in an orthogonal configuration. Connections to the microprocessor system, depending on the design of the converter, can also be made directly or using signal ribbon cables. To increase the interference immunity when connecting with ribbon cables, it is recommended to twist the pairs of the PWM signal with its GND. All PCBs layouts were designed using Autodesk Eagle software. Figure 6 shows the layout of PCBs taking into account the dimensions of individual components.

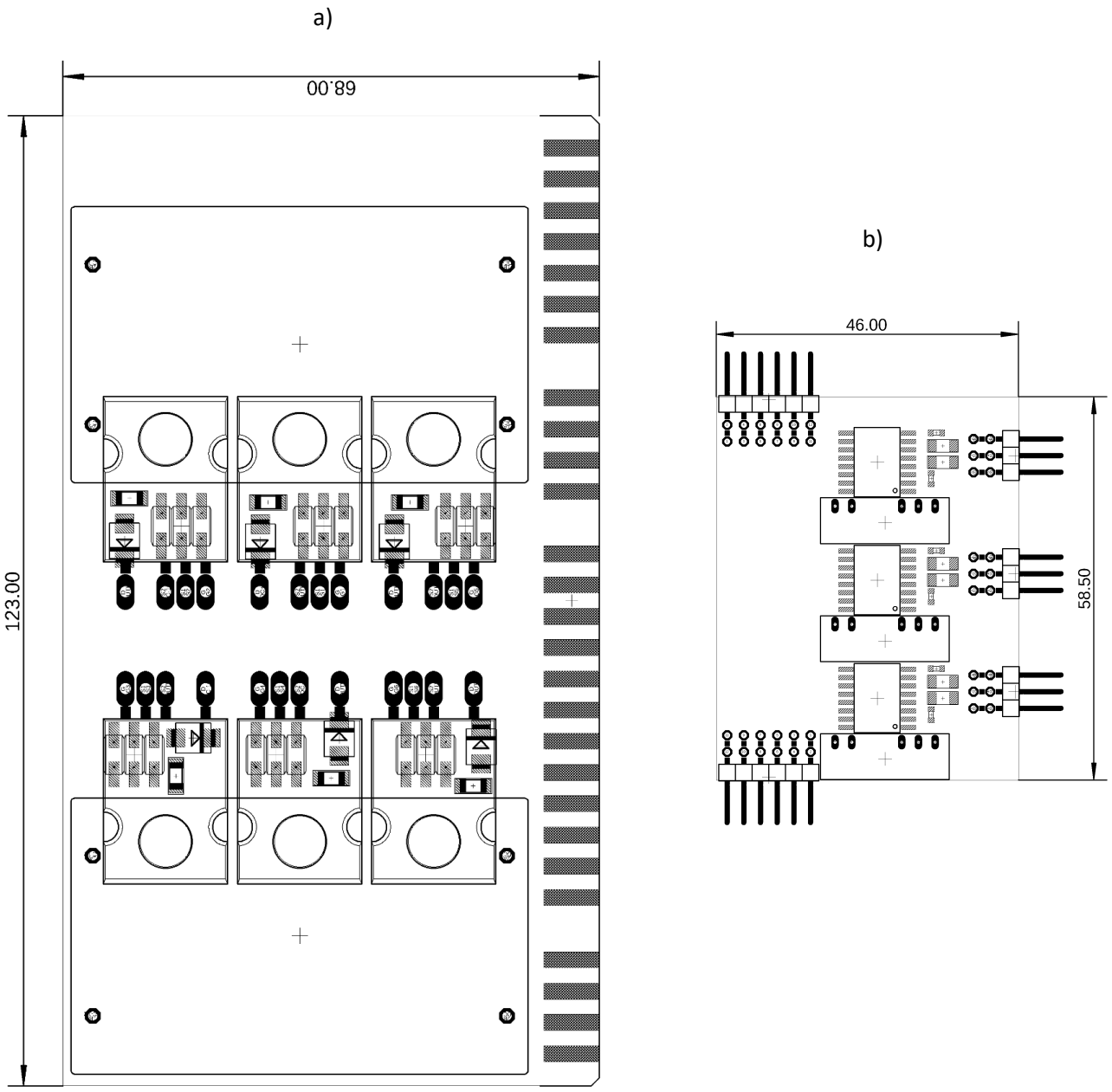


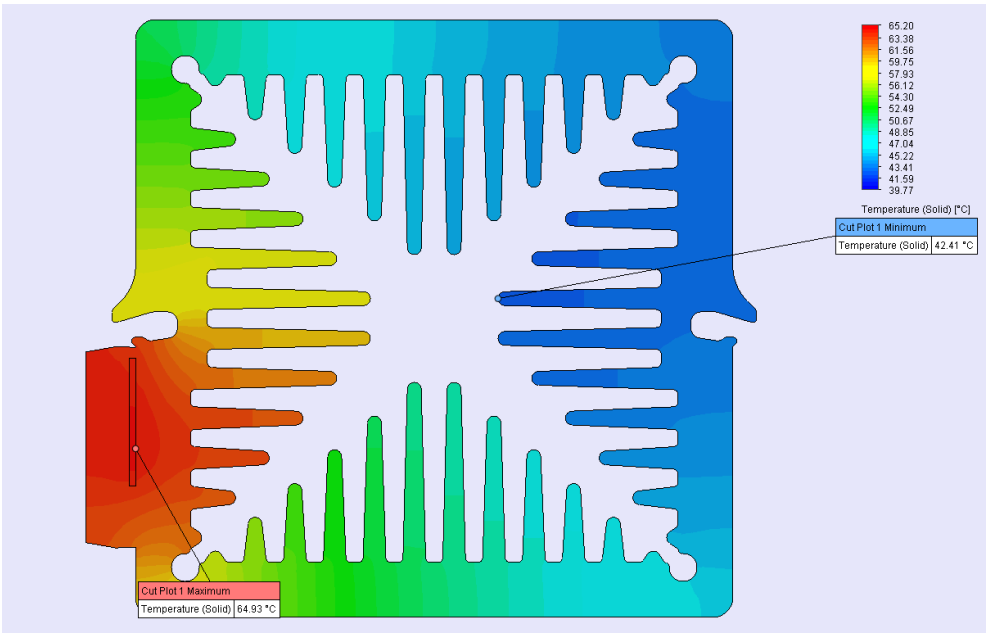
Figure 6. Layout of the a) power PCB and b) gate driver PCB

4. Thermal simulation

Appropriate thermal management of PES allows for reliable operation in the assumed lifetime of the solution. In order to determine the highest temperatures in the system, a thermal simulation was carried out.

The components listed in Table 1 for the PES cooling system (heatsink and fan) were selected in an iterative way through thermal simulations using the SolidWorks Flow tool. The power losses were assumed for the worst-case energy flow scenario. The results obtained for the final components are shown in Figure 6.

a)



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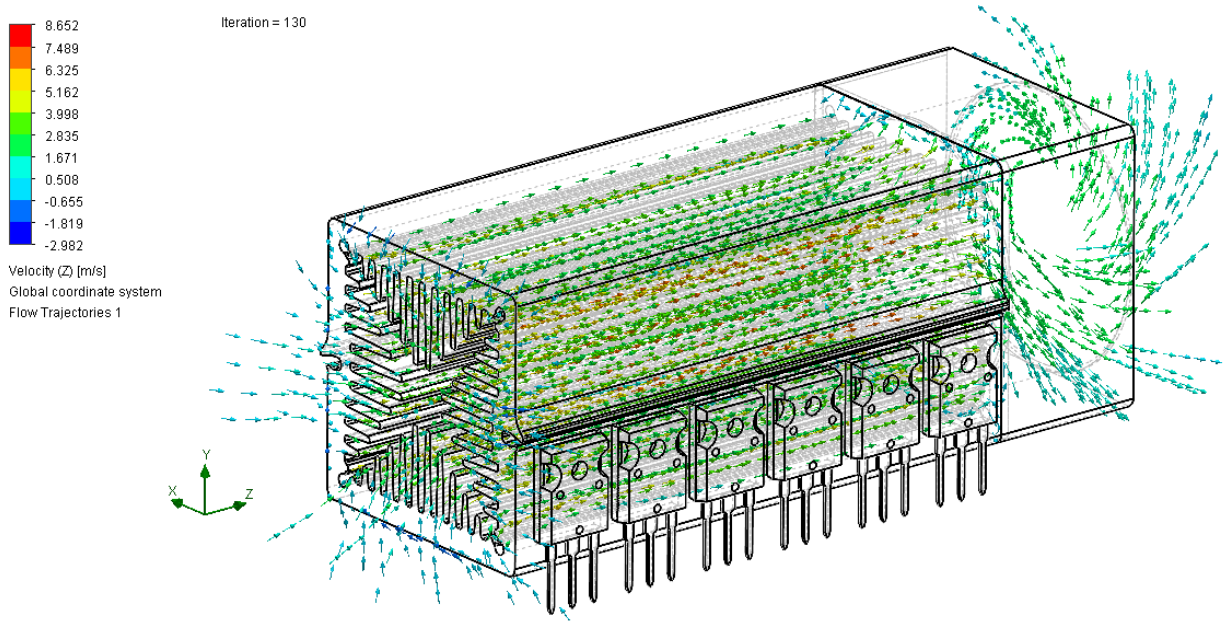

Figure 1. Thermal simulation of the cooling system: a) highest temperature point of the heat sink, b) airflow velocity

5. The layout of the Power Electronics Submodule

In the final phase of the Power Electronics Submodule design, all the component models were used to create a 3D model of the solution. Using the SolidWorks software, the exact layout of PES was modeled, and executive documentation was prepared. Figure 7 shows the view of the designed solution.

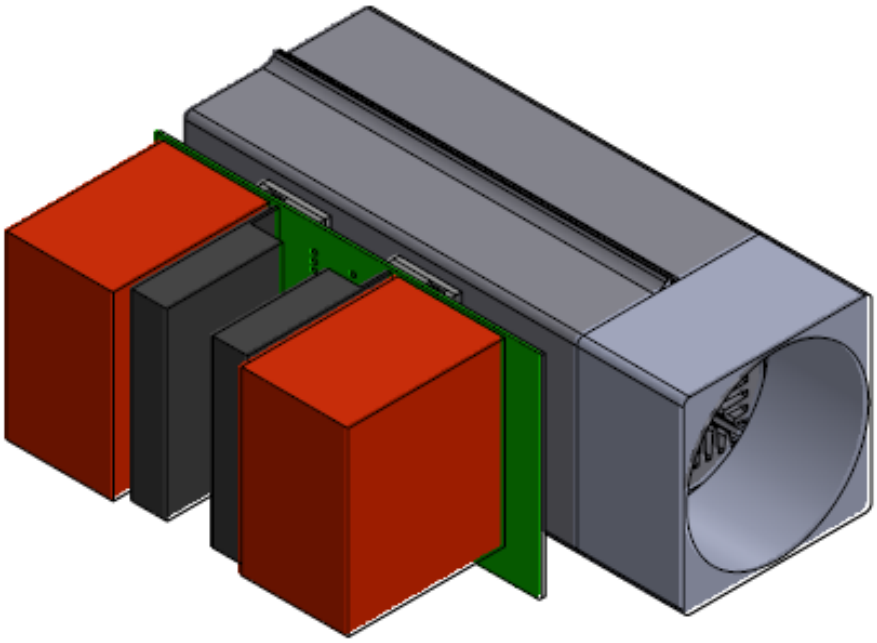

Figure 2. The layout of the 10 kW Power Electronic Submodule (PES) – a view of the 3D model

Power density is also an important parameter of modern converters. The PES layout was designed so that the dimensions of the solution met all the initial assumptions were compact. External dimensions of PES are presented in Figure 8.

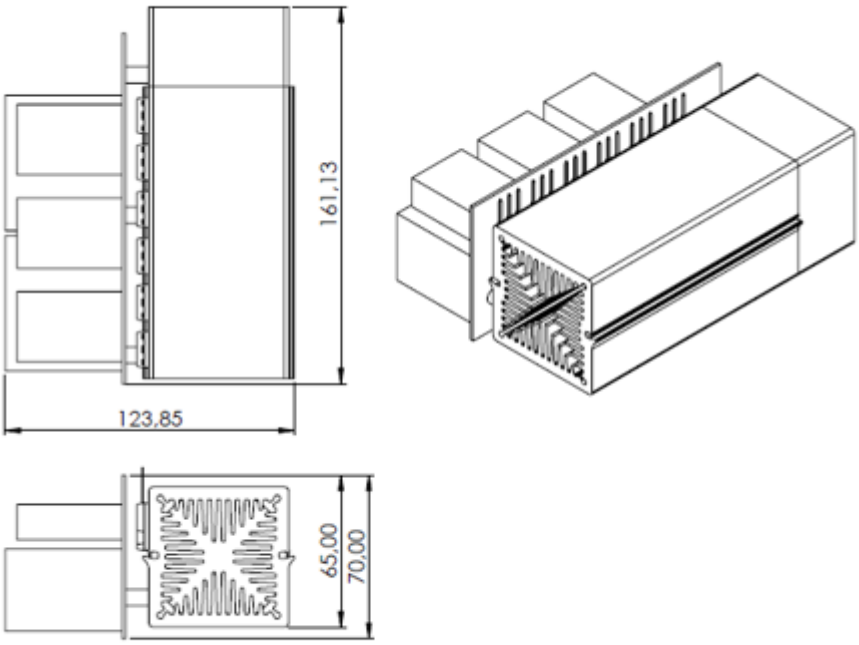

Figure 3. Dimensions of PES

6. Conclusions

Implementation of a Power Electronics Submodule that meets the requirements of all converters planned in the MoReSiC project is not a trivial problem. At all stages of PES design, special attention should be paid to minimizing parasitic inductances of the commutation circuit. This parameter is of key importance for the utility features of each converter. From the designer's point of view, the best results can be achieved by selecting components with low internal inductances and keeping the PES compact. However, one should not forget about the thermal characteristics of the device. The optimal design must consider the compromise between minimizing parasitic parameters and an efficient cooling system. External constraints such as component availability and cost of the components should also be kept in mind during project implementation.